LOONGSON

Loongson 1C 300 Processor DataSheet

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Loongson Technology Corporation Limited

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Revision history

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Feb. 28, 2013	R&D Center	V0.1	Internal preview version
Mar. 6, 2013	R&D Center	V0.1	Update corresponding contents of pin assignment change
Apr. 15, 2013	R&D Center	V0.2	Update multiplexing relationship
Apr. 24, 2013	R&D Center	V0.2	Amend clock and partial multiplexing description
Jun. 14, 2013	R&D Center	V0.3	Amend power supply descriptions
Feb. 28, 2014	R&D Center	V0.9	Amend changes in the second version
Apr. 21, 2014	R&D Center	V1.0	Add default multiplexing relationship and pull-up/pull-down descriptions Add SRAM pin description and some errors Update chip name as Loongson 1C300

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1. Overview

Loongson 1C300 (hereinafter referred to as 1C) chip is a cost-effective single chip system based on LS232 processor core, and is applicable to fields such as biological recognition of fingerprints and Internet of Things sensing.

1C includes the floating point processing unit, and can effectively enhance the processing ability of system floating point data. The memory interface of 1C supports several types of memories and allows the flexible system design. It supports 8-bit SLC NAND or MLC NAND FLASH, and provides the storage expansion interface of high capacity.

1C has provided various serial peripheral interfaces and on-chip modules for developers, including Camera controller, USB OTG 2.0 and USB HOST 2.0 interfaces, AC97/I2S controller, LCD controller, high-speed SPI interface, full-function UART interface, and owns the sufficient computing ability and multi-application connectivity.

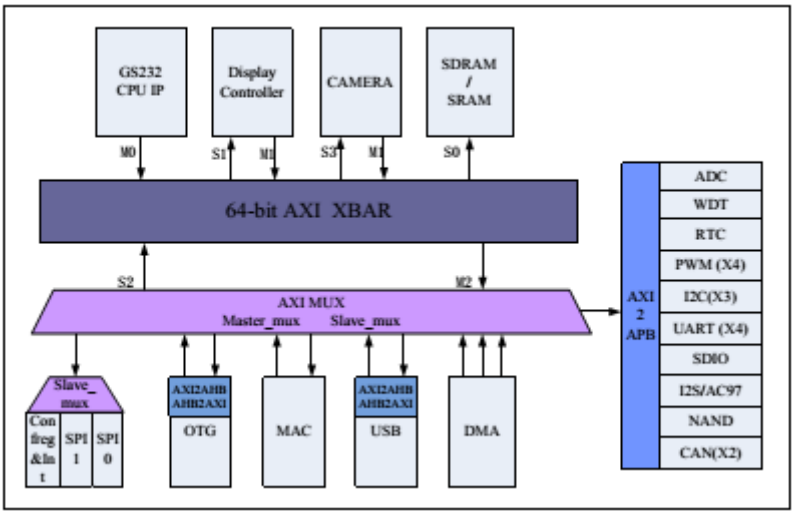


Figure 1-1 Structure chart of Loongson 1C

1.1 Chip characteristics

1.1.1 General characteristics

- Chip technology 0.13um CMOS
- Supply voltage I/O: 3.3 ±0.3V; processor core: 1.2 ±0.2V

(The IO pins are 5V tolerant)

- Package QFP100, 0.5 mm pitch
  QFP176, 0.4 mm pitch
- Operating frequency 300MHz
- Power dissipation ≤ 0.5W

1.1.2 Processor core

- Single core LS232, MIPS32 architecture compatible, and main frequency of 300MHZ.
- It supports the highly effective dual-issue technology (one clock tick executes two instructions)
- It supports the out-order issue and execution technologies such as register renaming, dynamic scheduling, and branch prediction
- 5-stage pipeline(instruction fetch, decode, issue, execution, write back and commit) micro-system structure
- 16KB data cache and 16KB instruction cache
- It integrates 64-bit floating point unit, supports the fully pipelining of 64-bit floating point additive and multiplying operations. Its hardware has accomplished the floating point division operation.

1.1.3 SDRAM controller

- SDRAM interface, operating frequency of 45-133MHz
- It supports the bus width of 8/16-bit parallel data.
- It supports the auto-refresh and self-refresh functions, and page mode.

1.1.4 SRAM/NOR FLASH controller

- SRAM and NOR Flash direct link interface, working frequency of 66-133MHz
- It supports the chip select pin of static memory, and can be configured separately.
- It supports the bus width of 8-bit/16-bit parallel data.

1.1.5 NAND controller

- It supports the single capacity of 4GB NAND FLASH at most
- It supports 512 bytes, 2K byte page and larger page FLASH
- Hardware ECC generation, detection and indication (software error correction)
- It supports the data reading speed of 8-10MB/S and writing speed of 5MB/s from Flash
- It supports the boot from NAND Flash
- It supports the mode of little endian

1.1.6 Clock generator

- 1. It has one standard PLL input interface, and supports the external crystal as chip clock input.
- It supports the on-chip output and can configure one way of clock for off-chip peripherals.
- PLL configurable frequency software

1.1.7 I^2S controller

- It supports the I^2S input in master mode
- It supports the I^2S output in master mode
- It supports the width of 8, 16, 18, 20, 24 and 32 bits
- It supports the audio data of mono and stereo
- It supports the sampling frequency of (16, 22.05, 32, 44.1 and 48)kHz
- It supports DMA transmission mode

1.1.8 AC97 controller

- Variable sampling rate AC97 coder and decoder interfaces (48KHz and below)
- It supports the stereo PCM and single-track MIC input
- It supports 2-channel stereo PCM output
- It supports the DMA and interrupt operation
- It supports 16, 18 and 20 bits sampling precision, and variable sampling rate.

- It supports 16 bits, and 16 entry FIFOs for each channel.

1.1.9 LCD controller

- It supports the 16/24-bit pixel mode
- It supports the display output of RGB444/555/565/888
- It supports the resolution of 1024x768, 800x600, 640 x 480 and 320 x 240
- It supports DMA transmission mode

1.1.10 Camera interface

- It supports ITU-R BT.601/656 8-bit input.
- It supports RAW RGB, RGB565 and YUV4:2:2 data input.
- It supports YUV, RGB888, RGB0888 and RGB565 output
- It supports the resolution scaling of 320x240 and 640x480
- It supports the resolution input of 2Kx2K at most, and the resolution can be configured.
- It supports DMA transmission mode

1.1.11 MAC controller

- It supports 10/100Mbps PHY device, including 10 Base-T, 100 Base-TX, 100Base-FX and 100 Base-T4;
- It's completely compatible with IEEE standard 802.3
- It's completely compatible with 802.3x full duplex flow control and half-duplex back pressure flow control
- It supports VLAN frames
- It supports DMA transmission mode
- It supports standard media independent interface (MII)
- It supports the standard Reduced Media Independent Interface (RMII), and may connect the external PHY chip.

1.1.12 USB2.0 controller

- One USB OTG2.0 controller
- One USB HOST 2.0 controller
- It supports the high-speed and full-speed mode
- It supports DMA transmission mode
- It's compatible with USB Rev 1.1 and USB Rev 2.0 protocols

1.1.13 SPI controller

- It supports two-way independent SPI interface, and each way of SPI interface supports four chip selects.
- Follow specifications of serial peripheral interface (SPI)
- Support synchronous, serial and full duplex communication
- Support SPI master mode
- Each transmission of 8-16 bits
- It supports inquiries and interrupt transmission mode
- It supports the SPI nor flash boot.
- It supports the SPI interface two-way input and output, and the maximum data transmission speed is 24-96 Mbps.
- It supports the minimum communication rate as low as 25KB, and facilitates the matching of special device.

1.1.14 I^2C controller

- Three-channel standard I2C bus interface
- It supports configuration of master, slave or master / slave mode
- Programmable bus clock frequency

1.1.15 UART controller

- It supports two full-function serial interfaces. Therein, the full-function serial interface 0 can be multiplexed as 4 two-wire serial interfaces, and support the smart card agreement.
- RxD0, TxD0, RxD1, TxD1, RxD2 and TxD2 based on interrupt operation;
- UART channel 0, 1 and 2 with IrDA 1.0
- UART channel 0 and 1 with RTS0, CTS0, RTS1 and CTS1

1.1.16 GPIO

- It supports 105 GPIO at most
- All GPIO (except boot and system configuration) is defaulted as input after reset
- All GPIO supports interrupt function
- Each GPIO pin supports the level-triggered and edge-triggered modes, and can be configured independently.
- GPIO pin rate up to 4MHz

1.1.17 PWM controller

- Four-way 32 bits can configure PWM timer.
- It supports the timer function
- It supports the counter function
- It supports the occurrence control in dead band prevention

1.1.18 RTC

- Timing is accurate to 0.1 second
- It supports the external crystal as RTC clock input.
- It supports the operation powered by external battery, and later by battery after powered off.
- The special power pin may be connected to the battery or 3.3V main power supply.
- Provide seconds, minutes, hours, days, months and years

1.1.19 CAN controller

- 2-channel independent CAN controller
- It's compatible with CAN2.0A and CAN2.0B protocols (the passive expansion frame in PCA82C200 compatible mode)
- It supports the CAN protocol extensions
- Bit rate is up to 1Mbits /s

1.1.20 SDIO controller

- 1-channel independent SDIO controller
- It's compatible with SD Memory 2.0/MMC/SDIO 2.0 protocol.
- Support SDIO boot

1.1.21 ADC controller

- Sampling rate up to 1MHz at most
- 4-channel ADC input
- Support 4-wire and 5-wire touch screens
- Support continuous sampling and single sampling

- Support analog watchdog

1.2 Document Conventions

1.2.1 Signal designation

The selection of the signal name complies with the principle of easy to remember and specify the identification function. Low desired signal is ended by n, and the high desired signal has no n. Without special instructions, the ACPI/GMAC/USB prefix signals are located in RSM domain, the prefix RTC signals in RTC domain, and other signals in SOC domain.

1.2.2 Signal type

Code	Description
A	Simulation
DIFF I/O	Two-way difference
DIFF IN	Difference input
DIFF OUT	Difference output
I	Input.
I/O	Two-way
O	Output
OD	Open-drain output
P	Power supply
G	Ground
PU	Pull up
PD	Pull down

1.2.3 Numeric representation

Hexadecimal number is expressed as ’hxxx, binary number ’bxx, and others decimal numbers.
The pins with the same function but different labels (such as DDR_DQ0, DDR_DQ1) is abbreviated by square brackets and numerical range (for example, DDR_DQ [63:0]) similarly, the register domain is also expressed in this way.

1.2.4 Register domain

Register is introduced in the form of [register name].[domain name]. For example, chip_config0.uart_split refers to the uart_split domain of chip configuration register 0 (chip_config0).

2 Pin Definition

2.1 LCD Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
LCD_CLK	O	PU	LCD clock signals	3.3V
LCD_HSYNC	O	PU	LCD horizontal synchronizing signal	3.3V
LCD_VSYNC	O	PU	LCD vertical synchronizing signal	3.3V
LCD_EN	O	PU	LCD enable signal	3.3V
LCD_DAT[15:0]	O	PU	LCD data signal	3.3V

[Notes] In QFP100 package, LCD interface can't be used. In QFP176 package, LCD may use 16bit and 24bit mode. In 16bit mode, the pin won't be multiplexed; in 24bit mode, the low bit needs to multiplex CAM_DAT [7:0] or MAC signal.

2.2 SDRAM Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
SD_CLK	O	-	SDRAM clock signal	3.3V
SD_CKE	O	-	SDRAM clock enable signal, effective high level	3.3V
SD_CSn	O	-	SDRAM chip select signal, low level active	3.3V
SD_RASn	O	-	SDRAM row strobe signal, low level active	3.3V
SD_CASn	O	-	SDRAM column strobe signal, low level active	3.3V
SD_WE	O	-	SDRAM read and write signals, low level for write	3.3V
SD_BA[1:0]	O	-	Bank signal of SDRAM, four banks in total	3.3V
SD_ADDR[12:0]	O	-	SDRAM address signal	3.3V
SD_DATA[15:0]	I/O	-	SDRAM data signal	3.3V
SD_DQM[1:0]	O		SDRAM data mask signals	3.3V

2.3 SRAM/NOR Flash Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
SRAM_CSn	O	-	SRAM chip select signal, low level active	3.3V
SRAM_WEn	O	-	SRAM writing enable signal, low level active	3.3V
SRAM_OEn	O	-	SRAM reading enable signal, low level active	3.3V
SRAM_ADDR[25:0]	O	-	SRAM address signal	3.3V
SRAM_DATA[15:0]	I/O	-	SRAM data signal	3.3V
SRAM_BHE	O		SRAM high Byte Data desired signal	3.3V
SRAM_BLE	O		SRAM low Byte Data desired signal	3.3V

[Notes] In QFP100 and QFP176 packages, SRAM/NOR Flash pin isn't bonded, and needs multiplexing with SDRAM, so SRAM/NOR Flash can't be used together with SDRAM. See Table 9-1 for multiplexing relation. Through the configuration of corresponding register, this group of

interface signals is multiplexed.

2.4 I²S Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
I2S_MCLK	O	PU	I2S clock signals	3.3V
I2S_BCLK	O	PU	I2S bit clock signal	3.3V
I2S_LRCK	O	PU	I2S channel selection signal	3.3V
I2S_DI	I	PU	I2S data serial input signal	3.3V
I2S_DO	O	PU	I2S data serial output signal	3.3V

[Notes] In QFP100 package, I2S interface isn't introduced, and needs to be multiplexed with MAC pin. In QFP176 package, I2S interface is introduced, and can be directly used.

2.5 I²C Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
I2C[2:0]_SCL	O	No introduction	I2C serial clock	3.3V
I2C[2:0]_SDA	I/O	No introduction	I2C serial data	3.3V

[Notes] In QFP100 and QFP176 packages, I2C interface isn't introduced, and needs to be multiplexed with MAC, EJTAG, LCD or CAM pin.

2.6 UART Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
UART0_TX	O	PU	UART0 data transmission	3.3V
UART0_RX	I	PU	UART0 data reception	3.3V
UART0_RTS	I	PU	UART0 reception request	3.3V
UART0_CTS	I	PU	UART0 reception permission	3.3V
UART0_DSR	I	PU	UART0 device ready	3.3V
UART0_DTR	O	PU	UART0 data terminal ready	3.3V
UART0_DCD	I	PU	UART0 carrier detect	3.3V
UART0_RI	I	PU	UART0 ringing tips	3.3V

[Notes] In QFP100 package, there is no full-function serial interface, and only two-wire type. In QFP176U package, the full-function serial interface can be directly used.

2.7 PWM Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
PWM0	O	PU	PMW0 output	3.3V
PWM1	O	PU	PMW1 output	3.3V
PWM2	O	No introduction	PMW2 output	3.3V
PWM3	O	No introduction	PMW3 output	3.3V

[Notes] In QFP100 package, PWM isn't introduced and needs to be multiplexed with others. In QFP176 package, PWM0 and PWM1 can be directly used, and PWM2 and PWM3 need to be multiplexed with others.

2.8 ADC Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
ADC_REXT	I	-	ADC reference resistance	25K Ohm

ADC_VREF	I	-	ADC reference voltage	0.5-0.9_VDDA
ADC_VDDA	I	-	ADC analog power supply	3.3V
ADC_VSSA	I	-	ADC analog ground	0
ADC_D0	I	-	ADC Channel Zero sampling input	0.01-0.99VREF
ADC_D1	I	-	ADC First Channel sampling input	
ADC_XP	I	-	The 2nd channel sampling input of touch screen X+/ADC	
ADC_YP	I	-	The third channel sampling input of touch screen Y+/ADC	

[Notes] The AD interface can only be used in QFP176A package.

2.9 SPI Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
SPI_SCK	O	PU	SPI clock output	3.3V
SPI[3:0]_CSn	O	PU	SPI chip select 0 to 3	3.3V
SPI_MOSI	O	PD	SPI data output	3.3V
SPI_MISO	I	PD	SPI data input	3.3V

2.10 EJTAG Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
EJTAG_SEL	I	PU	JTAG selects(0: JTAG, 1: EJTAG)	3.3V
JTAG_SEL	I	PU	TAG pin function multiplex (when the bit is 1, select the multiplex function)	3.3V
EJTAG_TCK	I	PU	JTAG clock	3.3V
EJTAG_TDI	I	PU	JTAG data input	3.3V
EJTAG_TMS	I	PU	JTAG mode	3.3V
EJTAG_TRST	I	PU	JTAG reset, to be pulled down	3.3V
EJTAG_TDO	O	PU	JTAG data output	3.3V

[Notes] Does EJTAG_SEL select JTAG or EJTAG? JTAG_SEL is used to choose JTAG multiplex function. Please don't be confused.

2.11 CAMERA Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
CAM_CLKOUT	O	PU	Camera reference clock output	3.3V
CAM_PCLK_I	I	PU	Camera pixel clock input	3.3V
CAM_HSYNC	I	PU	Camera horizontal synchronization signal	3.3V
CAM_VSYNC	I	PU	Camera vertical synchronizing signal	3.3V
CAMDATA[7:0]	I	PU	Camera data input	3.3V

[Notes] In QFP100 package, CAM isn't introduced and needs to be multiplexed with NAND and MAC. In QFP176 package, CAM can be directly used.

2.12 NAND Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
NAND_CLE	O	PD	NAND command latch	3.3V

NAND_ALE	O	PD	NAND address latch	3.3V
NAND_RD	O	PD	NAND read signal	3.3V
NAND_WR	O	PD	NAND write signal	3.3V
NAND_CE	O	PD	NAND chip select 0	3.3V
NAND_RDY	I	PD	NAND ready 0	3.3V
NAND_D [7:0]	I/O	PD	NAND address / data lines	3.3V

2.13 MAC Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
MAC_TXCK	O	PU	MII clock transmission	3.3V
MAC_TXEN	O	PU	MII control transmission	3.3V
MAC_TXD[3:0]	O	PU	MII data transmission	3.3V
MAC_RXCK	I	PU	MII clock reception	3.3V
MAC_RXDV	I	PU	MII control reception	3.3V
MAC_RXD[3:0]	I	PU	MII data reception	3.3V
MAC_MDCK	O	PU	SMA interface clock	3.3V
MAC_MDIO	I/O	PU	SMA interface data	3.3V
MAC_COL	I	PU	MAC collision detection	3.3V
MAC_CRS	I	PU	MAC carrier detect	3.3V

[Notes] In QFP package, MAC can only use RMII mode. In QFP176 package, MII and RMII modes can be used.

2.14 OTG Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
OTG_DVDD			OTG digital power	1.2V
OTG_DVSS			OTG digital ground	0
OTG_VDD33			OTG analog power supply	3.3V
OTG_VSS33			OTG analog ground	0
OTG_REXT			OTG reference resistor to ground	44.2 Ohm
OTG_DP	DIFF I/O	-	OTG differential signal line D +	5V
OTG_DM	DIFF I/O	-	OTG differential signal line D -	5V
OTG_VBUS			OTG_VBUS	5V
OTG_ID			OTG_ID	3.3V

2.15 USB Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
USB_DVDD			USB digital power	1.2V
USB_DVSS			USB digital ground	0
USB_VDD33			USB analog power supply	3.3V
USB_VSS33			USB analog ground	0
USB_REXT			USB reference resistor to ground	44.2 Ohm
USB_DP	DIFF I/O	-	USB differential signal line D +	5V
USB_DM	DIFF I/O	-	USB differential signal line D -	5V

[Notes] In QFP100 package, USB HOST can’t be used. In QFP176 package, it can be used.

2.16 RTC Interface

Signal name	Type	Pull-up/pull-down	Description	Voltage
RTC_CLK_I	I	-	RTC oscillator input, connect 32.768K oscillator	-
RTC_CLK_O	O	-	RTC oscillator output	-
VR_VDDA			RTC power supply	3.0V

2.17 Clock Configuration Signal

Signal name	Type	Pull-up/pull-down	Description	Voltage
XTALI	I	-	System clock oscillator input, connection with 24M	-
XTAL0	0	-	System clock oscillator output	-

2.18 Power Ground

Signal name	Type	Pull-up/pull-down	Description	Voltage
PLL_ VDD33	P		Core PLL analog power supply	3.3V
PLL_ VSS33	G		Core PLL analog ground	0
PLL_VDD12	P		Core PLL digital power supply	1.2V
PLL_VSS12	G		Core PLL digital ground	0
CORE_VDD	P		Core voltage power supply	1.2V
CORE_VSS	G		Core voltage ground	0
IO_VDD	P		IO power supply	3.3V

2.19 Initialization Signal

Loongson 1C has three starting methods: SPI FLASH, NAND FLASH and SDIO. Multiplex function pin obtains the configuration message from the pull-up and pull-down values during system reset for the software to judge the powered state.

Table 2-1 Configuration signals

Pin name	Signal name	Description
NAND_D [3:0]	start_freq	When powered on and booted, PLL is configured by frequency doubling, and CPU frequency is half of it (except bypass mode), SDRAM frequency half of CPU frequency. The frequency is calculated as follows: Freq = 6*(4*NAND_D[3:0] + 40); When NAND_D[3:0]=0, it's the bypass mode.
NAND_D [5:4]	boot_sel	In boot selection, it's different in QFP100 and QFP176 packages (under QEP100 package, NAND control signals aren't bonded into pin) from that under QFP100 package, and boot_sel is 01: it indicates the boot from SPI flash 10: it indicates the boot from NAND flash (multiplex SDRAM pin) 11: it indicates from NAND flash boot (multiplex MAC pin), in QFP176 package, boot_sel is 01: it indicates the boot from SPI flash 10: it indicates the boot from NAND flash 11: it indicates the boot from SDIO
NAND_D [7:6]	nand_type	In NAND boot, configure the particle capacity of NAND flash 11: it indicates the capacity is equal to 2Gb（2KB page/4KB page/8KB page） 10: it indicates that capacity is 1Gb (2KB page)

		01: it indicates that the capacity is 512Mb (512 Bytes page) 00: it indicates the capacity is low and equal to 256MB (512 Bytes page)
NAND_CLE	rs_rd_cfg	Whether ECC is adopted in NAND boot. It's only valid when boot_sel selects NAND flash boot. When the bit is 0, it indicates the NAND non-ECC boot. When the bit is 1, it indicates the NAND ECC boot.
SPI0_CLK	usb_refclksel	For the clock selection signal of USB_HOST and USB_OTG, when the bit is 1, the clock is provided by internal PLL. When the bit is 0, the clock is provided by external crystal oscillator. Must be pulled up.

3 Function Description

3.1 Description of SDRAM Controller Interface

Integrating the memory controller, Loongson 1C supports the common 8bit and 16bit SDRAM particles, and stores at least 256MB.

3.1.1 SDRAM controller characteristics

Loongson 1C processor has one memory controller, supports 2bit chip selection (not support all 1C1 packets), 14bit address bus (row/column multiplexing) and 2bit logic Bank address bus, realizes the maximum addressing unit of 1G(2^{30}) (1C1 is equal to 512M). If the data bit is 16bit wide, the maximum addressing space is 2GB (1C1 is equal to 1GB).

Before using SDRAM, it's necessary to set the parameters of SDRAM controller. For Loongson 1C processor, the maximum width of row address and column address supported by SDRAM controller is 14 and 13 respectively, and the logic bank signal is 2bit. Each determined row address, column address and bank address correspond to one and only memory cell, and the contents in each memory cell determine whether it's selected by DQM. It considers the address continuity of user memory and reduce the overhead of row changing. The mapping relation of physical address, line and column address is shown as follows:

Physical address= {cs, row, bank, col}* data width / 8

(Note: no CS in 1C1)

The memory controller receives the memory read and writes requests sent by processor or peripheral. No matter the read or write operation, the memory controller is in slave state.

The memory controller has realized the function of dynamic page management. When accessing the memory, no intervention of software designers is needed, and the controller will select the latest closed row and staggered pre-charge strategy. The memory controller characteristics include:

- Refresh and go into low power mode;
- Configure memory controller parameters via registers;
- Different bank write and read operations realize the fully pipelining;
- Frequency：33MHz-150MHz
- 8/16-bit selectable software bus width.

3.1.2 SDRAM basic reading timing sequence

Figure 3-1 shows the SDRAM read protocol, and commands (CMD) include RAS_n, CAS_n and WE_n. When a read request occurs, RAS_n=1, CAS_n=0, WE_n=1.

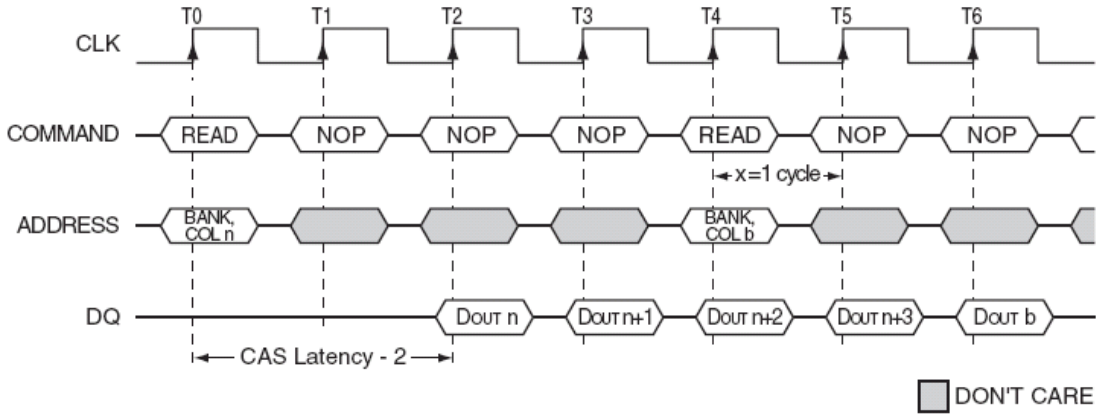


Figure 3-1 SDRAM read protocol

Note: Cas Latency = 2, Burst Length = 4

3.1.3 SDRAM basic writing timing sequence

Figure 3-2 shows the SDRAM writing protocol and commands (CMD) including RAS_n, CAS_n and WE_n. When a write request occurs, RAS_n=1, CAS_n＝0, WE_n＝0. Different from read protocol, DQM is used to mask write data.

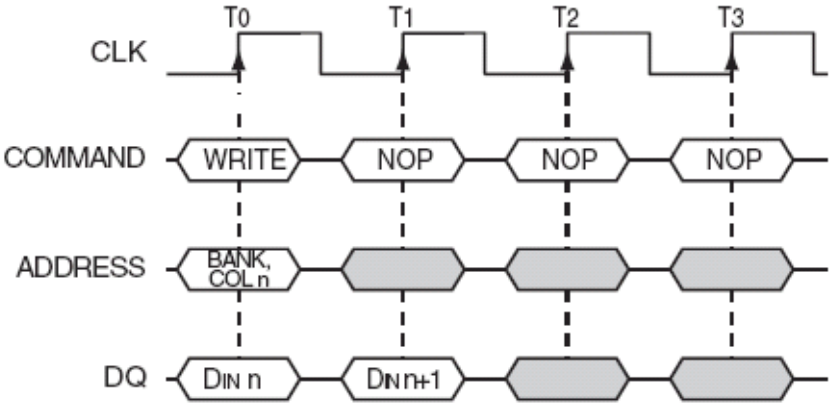


Figure 3-2 SDRAM write protocol

Note: Burst Length = 2.

3.2 Description of CAMERA Interface

Integrating the CAMERA interface, Loongson 1C supports ITU-R BT.601/656 YCbCr 8-bit standard and RGB565/888 8-bit standard transmission. It supports 640x480, 320x240 and any other resolution modes; it supports the scaling down by two in 640x480 resolution of RGB565\888 and ITU-R BT.601 modes, and the rest resolution doesn't support the function of scaling down; it supports the output in the format of YUV4:2:2/RGB565/RGB888/RGB0888.

3.2.1 Characteristics of CAMERA interface

Loongson processor includes one camera controller, scales down and converts the input image based on the register configuration. Controller characteristics include:

- It supports the external interface of ITU-R BT.601/656 8-bit and RGB565/RGB888 8-bit modes.
- Support configuration by any resolution input;
- Only 640x480 supports the scaling down by two.
- Output format: YCbCr 4:2:2, RGB565, RGB888 and RGB0888 (32bits). When the output format is RGB565/ YCbCr 4:2:2, the input pixels must be integral times of 32; the output format is RGB888/RGB0888, and the input pixel is integral times of 16.
- It supports the input of ITU-R BT.601/656 8-bit in any pixel into the output in the format of RGB (565/0888), and doesn't support the conversion of RGB input into YCbCr4:2:2 output;
- The output area has four sections, each of which can configure the address space of one frame image, and can configure the base address of address space, offset address of u and v component storage in the format of YCbCr4:2:2
- It supports the conversion of RGB565 into RGB565;
- It supports the conversion of RGB888 into RGB888 and RGB0888;
- It supports the conversion of BT601 into RGB565, RGB0888 and YUV;
- It supports the conversion of BT656 into RGB565, RGB0888 and YUV;
- It supports the 640 x 480 scaling down by two (except the format of TU-R BT.656);
- It supports the matrix display of the output in the format of RGB.

3.2.2 CAMERA interface protocol

Controller and Camera interface (CAMIF) signal
PCLK: 1bit input signal; Camera processor driven pixel clock.
VSYNC: 1bit input signal; Camera processor driven frame sync signal.
HREF: 1-bit input signal; Camera processor driven horizontal sync signal.
DATA: 8bit input signal; pixel data initiated by Camera processor.
ITU-R BT.601 8-bit input timing sequence is shown in Figure 3-3. Therein, the data input sequence may be YCbY Cr or YCrYCb or CrYCbY or CbYCrY.
RGB565/RGB888 8-bit input timing sequence and ITU-R BT.601 8-bit input timing sequence are consistent, and the data input sequence is different. For RGB888, the data input sequence may be R G B or B G R. For RGB565, the data input sequence may be R5G3 G3B5 or B5G3 G3R5. RGB565/RGB888 and ITU-R BT.601 input mode can set the line effective and frame effective high and low levels based on low two bits of status register.

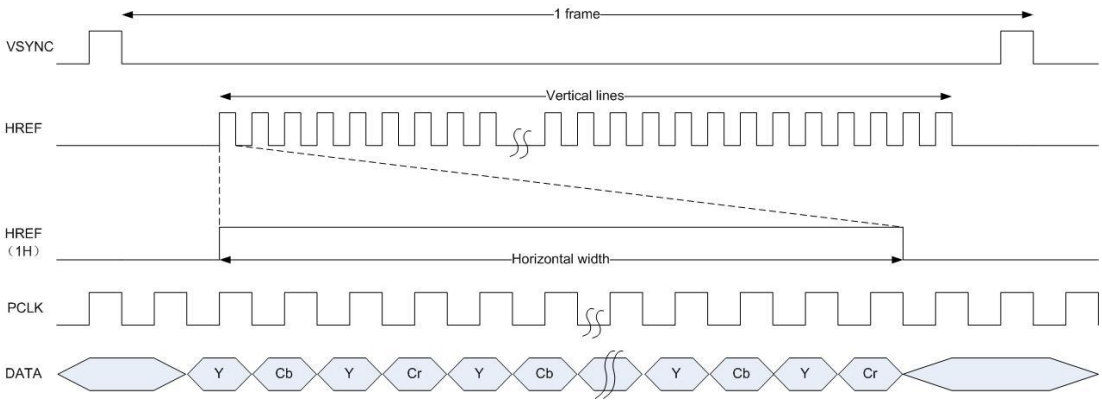


Figure 3-3 ITU-R BT.601 input timing sequence

ITU-R BT.656 input timing sequence is shown in Figure 3-4. Therein, the data input sequence can be Y CbYCr or YCrYCb or CrYCbY or CbYCrY. SAV is the line start code, and EAV is end code. The definition of reference code is shown in Table 3-, and the definition of XY value is shown in Table 3-. Only when XY is 80, 9D combination or C7, DA combination, it's effective line data.

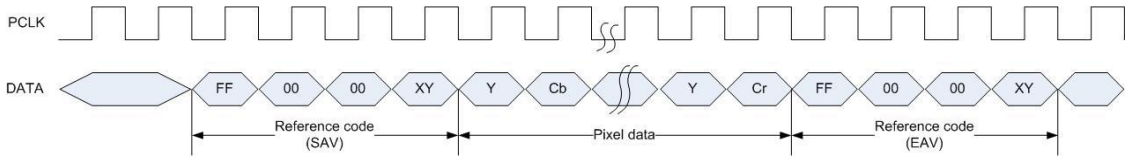


Figure 3-4 ITU-R BT.656 input timing sequence

Table 3-1 ITU-R BT.656 reference code

Data bit number	The first byte (3FF)	The second byte (000)	The third byte (000)	The fourth byte (XYZ)
7(MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0	1	0	0	P0

Note:
F 0 in field 1; 1 in field 2.
V 0 in other positions; 1 during field blanking interval
H 0 in SAV and 1 in EAV.
P0, P1, P2, P3: protection byte (see Table 3-)

Table 3-2 The fourth byte XY value

MSB							LSB	XY senary
1	F	V	H	P3	P2	P1	P0	
1	0	0	0	0	0	0	0	80
1	0	0	1	1	1	0	1	9D
1	0	1	0	1	0	1	1	AB
1	0	1	1	0	1	1	0	B6
1	1	0	0	0	1	1	1	C7
1	1	0	1	1	0	1	0	DA
1	1	1	0	1	1	0	0	EC
1	1	1	1	0	0	0	1	F1

3.3 Description of ADC Controller Interface

Integrating the ADC controller, Loongson 1C is used to control ADC channel and has realized some specific applications, such as continuous switch, single switch, touch screen application and analog watchdog.

3.3.1 Characteristics of A DC interface

Main characteristic parameters of ADC controller in Loongson 1C include:

- 4-channel ADC analog input, 10bit output precision
- Measuring voltage range is 0.15- 0.99VREF and it's recommended that the simulated input voltage doesn't exceed 3.3V.
- The operating frequency of ADC can be configured from 0 to 16M
- The operating mode of ADC has single and continuous switch, and the touch screen application belong to the special continuous switch.
- The continuous conversion of ADC adopts DMA transmission data, but the coordinates of touch screen doesn't adopt DMA.
- The continuous conversion interval of ADC can be configured from 0 to 1M.
- In continuous switch, the unused channels of ADC may conduct the single switch.
- In touch screen application, when the touch screen is pressed, the interrupt is generated; when the touch screen is released, the interrupt is also generated.
- It can support four-wire touch screen and five-wire touch screen. In the connection of four-wire touch screen, two ways of general ADC may be used. In the connection of five-wire touch screen, three ways of general ADC may be used.
- It supports multi-channel scanning single conversion
- It supports the function of analog watchdog, and the upper and lower thresholds may be configured. And the interrupt is generated when exceeding the threshold.

3.3.2 Touch screen application of ADC controller

The chip has four ways of ADC inputs in total, among which two ways are used for the sampling of touch screen (X and Y directions) and the rest two ways are general ADC input. ADC controller supports the four-wire and five-wire touch screens and their measuring methods are slightly different.
Measuring principles of four-wire touch screen are as follows:

Four-wire touch screen consists of two resistive layers. One layer has one vertical bus on right and left screen edges respectively, and the other layer has one horizontal bus on screen top and bottom. See the figure below. For the purpose of measurement in X direction, the left bus offset is 0V, and the right one is VRFF. Connect the top or bottom bus to ADC, and conduct one measurement when the top level meets the bottom one.
For the purpose of measurement in Y direction, the top bus offset is VRFF, and the bottom one is 0V. Connect the ADC input end to left bus or right bus, and conduct the voltage measurement when the top level meets the bottom one. Figure 3-5 has shown the simplified model when four-wire touch screen touches in two levels. For the four-wire touch screen, ideally connect the bus with the offset as VRFF to the positive reference input end of ADC, and connect the bus set to 0V to the positive reference input end of ADC.
In measuring the input of touch screen, except two ways of ADC inputs (X+ and Y+), two digital PAD (X- and Y-) pins need to be cooperated with.
In X-direction measurement, VREF and 0 are output in X+ and X- respectively, and the ADC conversion of Y+ is enabled at the same time; in Y-direction measurement, VREF and 0 are output in Y+ and Y- respectively, and the ADC conversion of X+ is enabled at the same time; in this way, the coordinates measurement is finished.

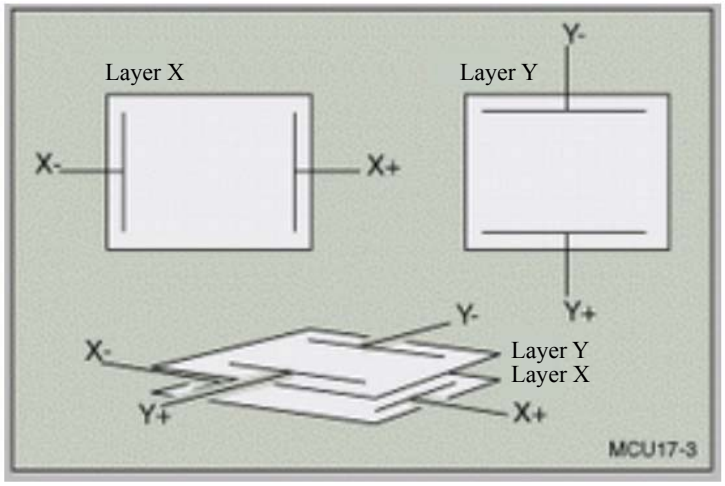


Figure 3-5 Measuring principles of touch screen

The principals of five-wire resistance screen measurement and four-wire measurement are basically the same, but slight different in measuring method.
The five-wire touch screen adopts one resistive layer and one conducting layer. The conducting layer has one contactor, which is always on one-side edge. Each touch spot is located in the four corners of the resistive layer. For the measurement in X axis, the top left and bottom left corners are offset to VREE, and the top right and bottom right are grounded. Because the voltage in right and left corners are the same, its effect is similar to that of the bus connecting right and left sides, like the method adopted in four-wire touch screen.
For the measurement in Y axis, the top left and top left corners are offset to VREE, and the bottom right and bottom right are grounded. Because the voltage in top and bottom corners are the same, its effect is similar to that of the bus connecting top and bottom edges, like the method adopted in four-wire touch screen. The advantage of this measuring algorithm is that the voltage in top left and bottom right remain unchanged. For the five-wire touch screen, ideally connect the top left (with the offset as VRFF) to the positive reference input end of ADC, and connect the bottom right (with the offset as 0V) to the negative reference input end of ADC.
In measuring the touch screen input, make one way of ADC input (Y+) cooperate with two digital PAD (X- and Y-) pins, connect LB (multiplexing X-) to the bottom left and RT (multiplexing Y-) to the top right, fix the top left to VREE and bottom right to 0V.
In X-direction measurement, VREF and 0 are output by bottom left and top right corners respectively, and the ADC conversion of Y+ is enabled at the same time; in Y-direction measurement, VREF and 0 are output by bottom left and top right respectively, and the ADC

conversion of Y+ is enabled at the same time; in this way, the coordinates measurement is finished.

4 Initialization Sequence

4.1 Power-on Sequence

1. RTC power supply VR_VDDA 3.0V, interval >1us
2. IO_VDD 3.3V, interval 1ms
3. PLL_VDD 3.3V, interval 1ms
4. CORE_VDD 1.2V

4.2 Reset Timing Sequence

At beginning, the SYS_RESET_ reset input is low, and is pulled up at least 10 milliseconds after the completion of power-on sequence.

5 Electrical Characteristics

5.1 Power Supply

5.1.1 Recommended operating conditions

Table 5-1 Recommended operating power supply voltage

Power supply	Description	Scope			Max current
		Min.	Typ.	Max.	
CORE_VDD	CPU domain power supply	1.1V	1.2V	1.3V	0.5A
IO_VDD	IO power supply	3.135V	3.3V	3.465V	TBD
VR_VDDA	RTC power supply	2.0V	3.0V	3.465V	100uA
ADC_VDDA	ADC analog power supply	3.135V	3.3V	3.465V	50mA
OTG_VDD33	OTG power supply	3.135V	3.3V	3.465V	50mA
OTG_DVDD	OTG power supply	1.1V	1.2V	1.3V	50mA
USB_VDD33	USB analog power supply	3.135V	3.3V	3.465V	50mA
USB_DVDD	USB analog power supply	1.1V	1.2V	1.3V	50mA
PLL_VDD33	PLL power supply	3.135V	3.3V	3.465V	50mA
PLL_DVDD	PLL power supply	1.1V	1.2V	1.3V	50mA

5.1.2 Absolute maximum rated value

Table 5-2 Absolute maximum rated value

Parameters	Description	Min	Max	Unit
CORE_VDD	CPU domain power supply	-0.2	1.3	V
IO_VDD	IO power supply	-0.3	3.46	V
VR_VDDA	RTC power supply	-0.3	3.46	V
OTG_VDD33	OTG power supply	-0.3	3.46	V
OTG_DVDD	OTG power supply	-0.3	1.2	V
USB_VDD33	USB analog power supply	-0.3	3.46	V
USB_DVDD	USB analog power supply	-0.3	1.2	V
PLL_VDD33	PLL power supply	-0.3	3.46	V
PLL_DVDD	PLL power supply	-0.3	1.2	V
Tstg	Storage temperature	-50	100	℃
Tw	Operating temperature	-40	80	℃

5.2 Characteristics of SDRAM Interface

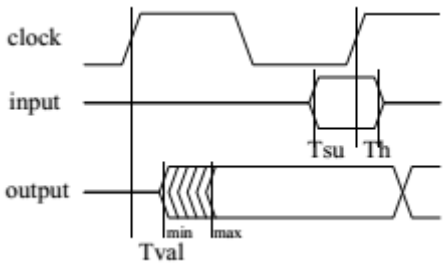


Table 5-3 Characteristics of SDRAM electrical AC timing sequence

Parameters	Symbol	Min	Generally	Max	Units
Input setup time	Tsu	0.9	-	-	ns
Input hold time	Th	3.5	-	-	ns
Output delay	Tval	1.1	-	4.26	ns

Notes: the above parameters are defined in chip pin, and the clock refers to SD_CLK.

5.3 Characteristics of CAMERA Interface

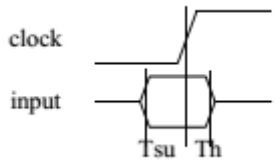


Table 5-4 Characteristics of CAMERA electrical AC timing sequence

Parameters	Symbol	Min	Generally	Max	Units
Input setup time	Tsu	2	-	-	ns
Input hold time	Th	1	-	-	ns

5.4 Characteristics of MAC Interface

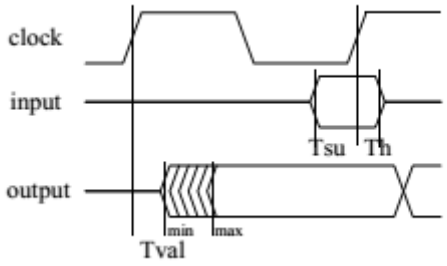


Table 5-5 Characteristics of MAC electrical AC timing sequence

Parameters	Symbol	Min	Generally	Max	Units
Input setup time	Tsu	10	-	-	ns
Input hold time	Th	10	-	-	ns
Output delay	Tval	0	-	11	ns

Notes: the above parameters have been defined by chip pin, and the RX and RX correspond to MAC_TXC and MAC_RXC in MII mode and MAC_TXC in RMII mode.

5.5 Characteristics of USB Interface

The table below sources from USB2.0 specification.

Table 5-6 USB DC electrical characteristics

Parameter	Symbol	Conditions	Min.	Max.	Units
InputLevelsforLow-/full-speed:					
High(driven)	VIH		2		V
High(floating)	VIHZ		2.7	3.6	V
Low	VIL			0.8	V
Differential Input Sensitivity	VDI	|(D+)-(D-)|	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	V
Input Levels for High-speed:					

High-speed squelch detection threshold (differential signal amplitude)	VHSSQ		100	150	mV
High speed disconnect detection threshold (differential signal amplitude)	VHSDSC		525	625	mV
High-speed differential input signaling levels					
High-speed data signaling common mode voltage range(guide line for receiver)	VHSCM		-50	500	mV
Output Levels for Low-/full-speed:					
Low	VOL		0	0.3	V
High(Driven)	VOH		2.8	3.6	V
SE1	VOSE1		0.8		V
Output Signal Crossover Voltage	VCRS		1.3	2	V
Output Levels for High-speed:					
High-speed idle level	VHSOI		-10	10	mV
High-speed data signaling high	VHSOH		360	440	mV
High-speed data signaling low	VHSOL		-10	10	mV
Chirp J level(differential voltage)	VCHIRPJ		700	1100	mV
Chirp K level(differential voltage)	VCHIRPK		-900	-500	mV
Decoupling Capacitance:					
Downstream Facing Port Bypass Capacitance (perhub)	CHPB	VBUS to GND	120		μF
Upstream Facing Port Bypass Capacitance	CRPB	VBUS to GND	1	10	μF
Input Capacitance for Low-/full-speed:					
Downstream Facing Port	CIND			150	pF
Upstream Facing Port(w/ocable)	CINUB			100	pF
Transceiver edge rate control capacitance	CEDGE			75	pF
InputImpedanceforHigh-speed:					
TDRspecforhigh-speedtermination					
Terminations:					
Bus Pull-up Resistoron Upstream Facing Port	RPU	1.5kΩ ±5%	1.425	1.575	kΩ
Bus Pull-down Resistoron Downstream Facing Port	RPD	15kΩ ±5%	14.25	15.75	kΩ
Input impedance exclusive of pullup/pulldown(forlow-/full-speed)	ZINP		300		kΩ

Termination voltage for upstream facing port pullup(RPU)	VTERM		3	3.6	V
Terminations in High-speed:					
Termination voltage in high-speed	VHSTERM		-10	10	mV

Table 5-7 USB HS source electrical characteristics

Parameter	Symbol	Conditions	Min.	Max.	Units
Driver Characteristics:					
Rise Time(10%-90%)	THSR		500		ps
Fall Time(10%-90%)	THSF		500		ps
Driver waveform requirements					
Driver Output Resistance(which also serves as high-speed termination)	ZHSDRV		40.5	49.5	Ω
Clock Timings:					
High-speed Data Rate	THSDRAT		479.76	480.24	Mb/s
Micro frame Interval	THSFRAM		124.9375	125.0625	μs
Consecutive Micro frame Interval Difference	THSRFI			4 high-speed bit times	
High-speed Data Timings:					
Data source jitter		Source and receiver jitter specified by the eye pattern templatesin Section7.1.2.2			
Receiver jitter tolerance					

Table 5-8 USB full-speed source electrical characteristics

Parameter		Symbol	Conditions	Min.	Max.	Units
Driver Characteristics:						
Rise Time		TFR		4	20	ns
Fall Time		TFF		4	20	ns
Differential Rise and Fall Time Matching		TFRFM	(TFR/TFF)	90	111.11	%
Driver Output Resistance for driver which is not high-speed capable		ZDRV		28	44	Ω
Clock Timings:						
Full-speed Data Rate for hubs and devices which are high-speed capable		TFDRATHS	Average bit rate	11.994	12.006	Mb/s
Full-speed Data Rate for devices which are not high-speed capable		TFDRATE	Average bit rate	11.97	12.03	Mb/s
Frame Interval		TFRAME		0.9995	1.0005	ms
Consecutive Frame Interval Jitter		TRFI	No clock adjustment		42	ns
Full-speed Data Timings:						
Source Jitter Total(including frequency tolerance):	To Next Transition	TDJ1		-3.5	3.5	ns
	For Paired Transitions	TDJ2		-4	4	ns
Source Jitter for Differential Transition to SE0 Transition		TFDEOP		-2	5	ns

Receiver Jitter:	To Next Transition	TJR1		-18.5	18.5	ns
	For Paired Transitions	TJR2		-9	9	ns
Source SE0 interval of EOP		TFEOPT		160	175	ns
Receiver SE0 interval of EOP		TFEOPR		82		ns
Width of SE0 interval during differential transition		TFST			14	ns

Table 5-9 USB low-speed source electrical characteristics

Parameter		Symbol	Min.	Max.	Units
Driver Characteristics:					
Transition Time:	Rise Time	TLR	75	300	ns
	Fall Time	TLF	75	300	ns
Rise and Fall Time Matching		TLRFM	80	125	%
Upstream Facing Port(w/cable, low-speed only)		CLINUA	200	450	pF
Clock Timings:					
Low-speed Data Rate for hubs which are high-speed capable		TLDRATHS	1.49925	1.50075	Mb/s
Low-speed Data Rate for devices which are not high-speed capable		TLDRATE	1.4775	1.5225	Mb/s
Low-speed Data Timings:					
Upstream facing port source Jitter Total(including frequency tolerance):	To Next Transition	TUDJ1	-95	95	ns
	For Paired Transitions	TUDJ2	-150	150	ns
Upstream facing port source Jitter for Differential Transition to SE0 Transition		TLDEOP	-40	100	ns
Upstream facing port differential Receiver Jitter:	To Next Transition	TDJR1	-75	75	ns
	For Paired Transitions	TDJR2	-45	45	ns
Downstream facing port source Jitter Total(including frequency tolerance):	To Next Transition	TDDJ1	-25	25	ns
	For Paired Transitions	TDDJ2	-14	14	ns
Downstream facing port source Jitter for Differential Transition to SE0 Transition					ns
Downstream facing port Differential Receiver Jitter:	To Next Transition	TUJR1	-152	152	ns
	For Paired Transitions	TUJR2	-200	200	ns
Source SE0 interval of EOP		TLEOPT	1.25	1.5	μs
Receiver SE0 interval of EOP		TLEOPR	670		ns
Width of SE0 interval during differential transition		TLST		210	ns

6 Pin Permutation and Package

In different applications, Loongson 1C has three packages: QFP100, QFP176A and QFP176U. Therein, QFP176A package supports ADC interface, and QFP176U package supports the full-function serial UART.

6.1 Package Pin According to the Pin Permutation

6.1.1 Package pin of QFP100

QFP100 package pin table is as follows:

Table 6-1 QFP100 package pin table ranked by pin

Pin Number	Net Name	Pin Number	Net Name	Pin Number	Net Name
1	XTALI	35	SD_A12	69	NAND_D2
2	XTALO	36	SD_A11	70	NAND_D1
3	LCD_CLK	37	SD_A10	71	NAND_D0
4	LCD_EN	38	SD_A09	72	CORE_VDD
5	SD_D15	39	SD_A08	73	SYS_RESET_
6	SD_D14	40	CORE_VDD	74	JTAG_FUNC_SEL
7	SD_D13	41	IO_VDD	75	IO_VDD
8	SD_D12	42	SD_A07	76	MAC_TXEN
9	SD_D11	43	SD_A06	77	MAC_TXD0
10	IO_VDD	44	SD_A05	78	MAC_TXD1
11	SD_D10	45	SD_A04	79	MAC_RXER
12	SD_D09	46	SD_A03	80	MAC_RXDV
13	SD_D08	47	SD_A02	81	MAC_RXD0
14	CORE_VSS	48	SD_A01	82	MAC_RXD1
15	SD_DQM1	49	SD_A00	83	MAC_TXC
16	CORE_VDD	50	CORE_VSS	84	OTG_DVSS
17	SD_DQM0	51	SPI0_MISO	85	OTG_DVDD
18	SD_D07	52	SPI0_MOSI	86	OTG_VDD33
19	SD_D06	53	SPI0_CS0	87	OTG_VSS33
20	SD_D05	54	SPI0_CLK	88	OTG_DM
21	SD_D04	55	EJTAG_FUNC_SEL	89	OTG_DP
22	SD_D03	56	EJTAG_TCK	90	OTG_REXT
23	SD_D02	57	EJTAG_TMS	91	OTG_VBUS
24	SD_D01	58	EJTAG_TDO	92	OTG_ID
25	SD_D00	59	EJTAG_TDI	93	CORE_VSS
26	SD_WE	60	EJTAG_RST	94	PLL_VSS12
27	SD_CASn	61	CORE_VDD	95	PLL_VDD12
28	SD_RASn	62	IO_VDD	96	PLL_VSS33
29	SD_CSn	63	CORE_VSS	97	PLL_VDD33
30	SD_BA1	64	NAND_D7	98	RTC_CLK_I
31	CORE_VSS	65	NAND_D6	99	RTC_CLK_O
32	SD_BA0	66	NAND_D5	100	VR_VDDA
33	SD_CKE	67	NAND_D4		
34	SD_CLK	68	NAND_D3		

6.1.2 QFP176A package pin

QFP176A package pin table is as follows:

Table 6-2 QFP176A package pin table according to the pin permutation

Pin Number	Net Name	Pin Number	Net Name	Pin Number	Net Name
1	XTALI	46	SD_WE	91	SPI0_MOSI
2	XTALO	47	SD_CASn	92	SPI0_CS0
3	LCD_CLK	48	SD_RASn	93	SPI0_CS1
4	LCD_HSYNC	49	SD_CSn	94	SPI_CLK
5	LCD_VSYNC	50	SD_BA1	95	EJTAG_FUNC_SEL
6	LCD_EN	51	CORE_VSS	96	EJTAG_TCK
7	LCD_DAT0	52	SD_BA0	97	EJTAG_TMS
8	LCD_DAT1	53	SD_CKE	98	EJTAG_TDO
9	LCD_DAT2	54	SD_CLK	99	EJTAG_TDI
10	LCD_DAT3	55	SD_A12	100	EJTAG_RST
11	CORE_VDD	56	SD_A11	101	CORE_VDD
12	LCD_DAT4	57	SD_A10	102	IO_VDD
13	LCD_DAT5	58	SD_A09	103	CAMDATA7
14	LCD_DAT6	59	SD_A08	104	CAMDATA6
15	LCD_DAT7	60	SD_A07	105	CAMDATA5
16	LCD_DAT8	61	SD_A06	106	CAMDATA4
17	LCD_DAT9	62	SD_A05	107	CAMDATA3
18	IO_VDD	63	SD_A04	108	CAMDATA2
19	LCD_DAT10	64	SD_A03	109	CAMDATA1
20	LCD_DAT11	65	SD_A02	110	CAMDATA0
21	LCD_DAT12	66	SD_A01	111	CORE_VSS
22	CORE_VSS	67	SD_A00	112	CAM_HSYNC
23	LCD_DAT13	68	CORE_VDD	113	CAM_VSYNC
24	LCD_DAT14	69	IO_VDD	114	CAM_CLKOUT
25	LCD_DAT15	70	I2S_DI	115	CAM_PCLK_I
26	CORE_VDD	71	I2S_DO	116	NAND_D7
27	SD_D15	72	I2S_LRCK	117	NAND_D6
28	SD_D14	73	I2S_BCLK	118	NAND_D5
29	SD_D13	74	I2C_SDA0	119	NAND_D4
30	SD_D12	75	I2C_SCL0	120	NAND_D3
31	SD_D11	76	I2S_MCLK	121	NAND_D2
32	SD_D10	77	URT0_RX	122	NAND_D1
33	SD_D09	78	URT0_TX	123	NAND_D0
34	SD_D08	79	URT0_RTS	124	CORE_VDD
35	SD_DQM1	80	URT0_CTS	125	SYS_RESET_
36	SD_DQM0	81	URT0_DSR	126	JTAG_FUNC_SEL
37	SD_D07	82	URT0_DTR	127	NAND_RDY
38	SD_D06	83	URT0_DCD	128	NAND_CLE
39	SD_D05	84	URT0_RI	129	NAND_ALE
40	SD_D04	85	PWM1	130	NAND_RD
41	SD_D03	86	PWM0	131	IO_VDD
42	SD_D02	87	SPI0_CS2	132	NAND_CE
43	SD_D01	88	CORE_VSS	133	NAND_WR
44	SD_D00	89	SPI0_CS3	134	MAC_TXEN
45	IO_VDD	90	SPI0_MISO	135	MAC_TXD0

Table 6-2 QFP176A package pin table according to the pin permutation

Pin Number	Net Name	Pin Number	Net Name	Pin Number	Net Name
136	MAC_TXD1	150	MAC_RXC	164	USB_DVDD
137	MAC_RXER	151	MAC_CRS	165	USB_VDD33
138	MAC_RXDV	152	CORE_VDD	166	USB_VSS33
139	MAC_RXD0	153	OTG_DVSS	167	USB_DM
140	MAC_RXD1	154	OTG_DVDD	168	USB_REXT
141	MAC_MDC	155	OTG_VDD33	169	USB_DP
142	CORE_VSS	156	OTG_VSS33	170	PLL_VSS12
143	MAC_MDIO	157	OTG_DM	171	PLL_VDD12
144	MAC_RXD2	158	OTG_DP	172	PLL_VSS33
145	MAC_TXD2	159	OTG_REXT	173	PLL_VDD33
146	MAC_RXD3	160	OTG_VBUS	174	RTC_CLK_I
147	MAC_TXD3	161	OTG_ID	175	RTC_CLK_O
148	MAC_TXC	162	CORE_VSS	176	VR_VDDA
149	MAC_COL	163	USB_DVSS		

6.1.3 QFP176U package pin

QFP176U package pin table is as follows:

Table 6-3 QFP176U package pin table according to the pin permutation

Pin Number	Net Name	Pin Number	Net Name	Pin Number	Net Name
1	XTALI	27	SD_D15	53	SD_CKE
2	XTALO	28	SD_D14	54	SD_CLK
3	LCD_CLK	29	SD_D13	55	SD_A12
4	LCD_HSYNC	30	SD_D12	56	SD_A11
5	LCD_VSYNC	31	SD_D11	57	SD_A10
6	LCD_EN	32	SD_D10	58	SD_A09
7	LCD_DAT0	33	SD_D09	59	SD_A08
8	LCD_DAT1	34	SD_D08	60	SD_A07
9	LCD_DAT2	35	SD_DQM1	61	SD_A06
10	LCD_DAT3	36	SD_DQM0	62	SD_A05
11	CORE_VDD	37	SD_D07	63	SD_A04
12	LCD_DAT4	38	SD_D06	64	SD_A03
13	LCD_DAT5	39	SD_D05	65	SD_A02
14	LCD_DAT6	40	SD_D04	66	SD_A01
15	LCD_DAT7	41	SD_D03	67	SD_A00
16	LCD_DAT8	42	SD_D02	68	CORE_VDD
17	LCD_DAT9	43	SD_D01	69	IO_VDD
18	IO_VDD	44	SD_D00	70	I2S_DI

19	LCD_DAT10	45	IO_VDD	71	I2S_DO
20	LCD_DAT11	46	SD_WE	72	I2S_LRCK
21	LCD_DAT12	47	SD_CASn	73	I2S_BCLK
22	CORE_VSS	48	SD_RASn	74	I2C_SDA0
23	LCD_DAT13	49	SD_CSn	75	I2C_SCL0
24	LCD_DAT14	50	SD_BA1	76	I2S_MCLK
25	LCD_DAT15	51	CORE_VSS	77	PWM1
26	CORE_VDD	52	SD_BA0	78	PWM0

Table 6-3 QFP176U package pin table according to the pin permutation (continued)

Pin Number	Net Name	Pin Number	Net Name	Pin Number	Net Name
79	SPI0_CS2	112	CAM_HSYNC	145	MAC_TXD2
80	CORE_VSS	113	CAM_VSYNC	146	MAC_RXD3
81	ADC_REXT	114	CAM_CLKOUT	147	MAC_TXD3
82	ADC_VREF	115	CAM_PCLK_I	148	MAC_TXC
83	ADC_VDDA	116	NAND_D7	149	MAC_COL
84	ADC_VSSA	117	NAND_D6	150	MAC_RXC
85	ADC_D0	118	NAND_D5	151	MAC_CRS
86	ADC_D1	119	NAND_D4	152	CORE_VDD
87	ADC_XP	120	NAND_D3	153	OTG_DVSS
88	ADC_YP	121	NAND_D2	154	OTG_DVDD
89	SPI0_CS3	122	NAND_D1	155	OTG_VDD33
90	SPI0_MISO	123	NAND_D0	156	OTG_VSS33
91	SPI0_MOSI	124	CORE_VDD	157	OTG_DM
92	SPI0_CS0	125	SYS_RESET_	158	OTG_DP
93	SPI0_CS1	126	JTAG_FUNC_SEL	159	OTG_REXT
94	SPI_CLK	127	NAND_RDY	160	OTG_VBUS
95	EJTAG_FUNC_SEL	128	NAND_CLE	161	OTG_ID
96	EJTAG_TCK	129	NAND_ALE	162	CORE_VSS
97	EJTAG_TMS	130	NAND_RD	163	USB_DVSS
98	EJTAG_TDO	131	IO_VDD	164	USB_DVDD
99	EJTAG_TDI	132	NAND_CE	165	USB_VDD33
100	EJTAG_RST	133	NAND_WR	166	USB_VSS33
101	CORE_VDD	134	MAC_TXEN	167	USB_DM
102	IO_VDD	135	MAC_TXD0	168	USB_REXT
103	CAMDATA7	136	MAC_TXD1	169	USB_DP
104	CAMDATA6	137	MAC_RXER	170	PLL_VSS12
105	CAMDATA5	138	MAC_RXDV	171	PLL_VDD12
106	CAMDATA4	139	MAC_RXD0	172	PLL_VSS33
107	CAMDATA3	140	MAC_RXD1	173	PLL_VDD33
108	CAMDATA2	141	MAC_MDC	174	RTC_CLK_I
109	CAMDATA1	142	CORE_VSS	175	RTC_CLK_O
110	CAMDATA0	143	MAC_MDIO	176	VR_VDDA
111	CORE_VSS	144	MAC_RXD2		

6.2 Top Pin Permutation

6.2.1 QFP100 top pin permutation

QFP100 top pin permutation is shown in the figure below

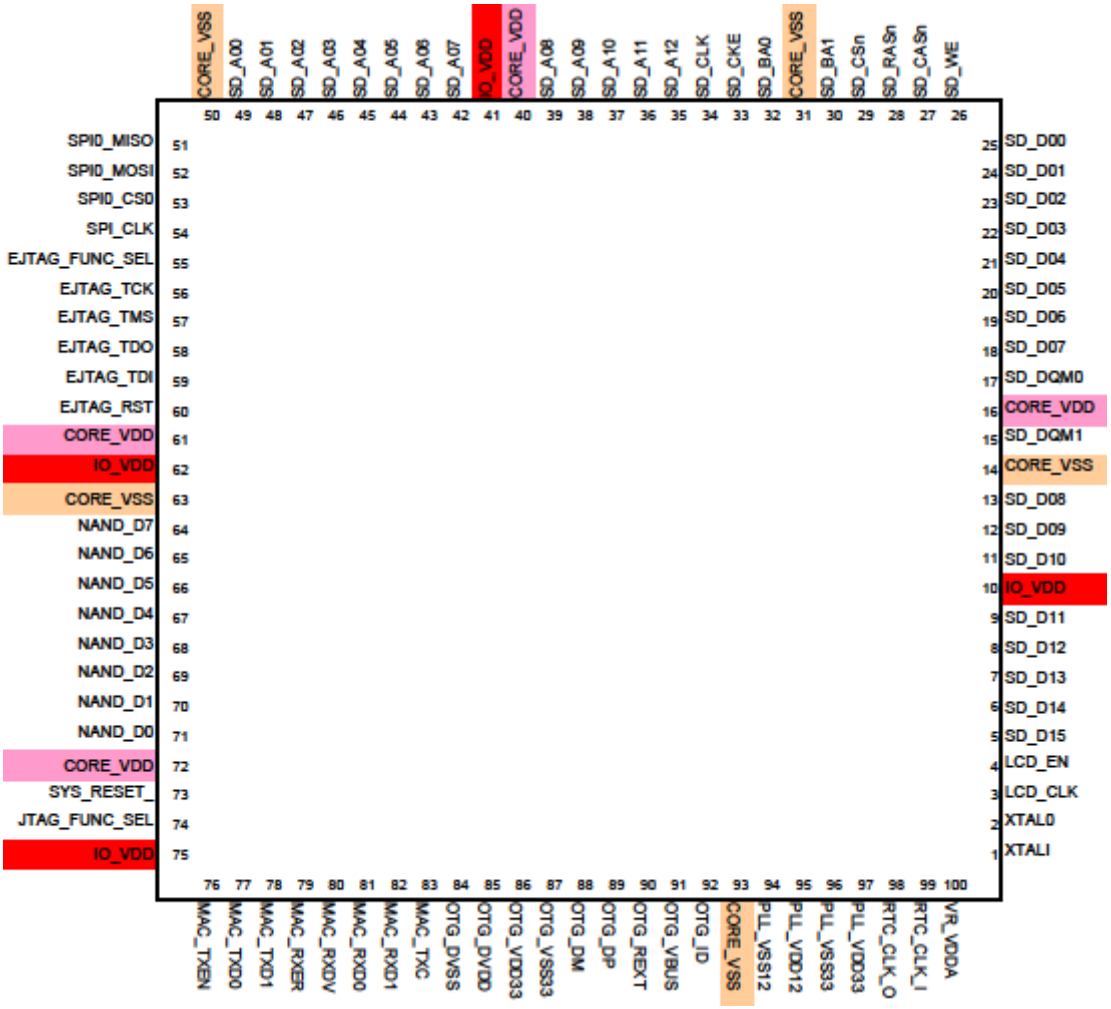


Figure 6-1 QFP100 top pin permutation

6.2.2 QFP176A top pin permutation

QFP176A top pin permutation is shown in Figure 6-2 and 6-3.

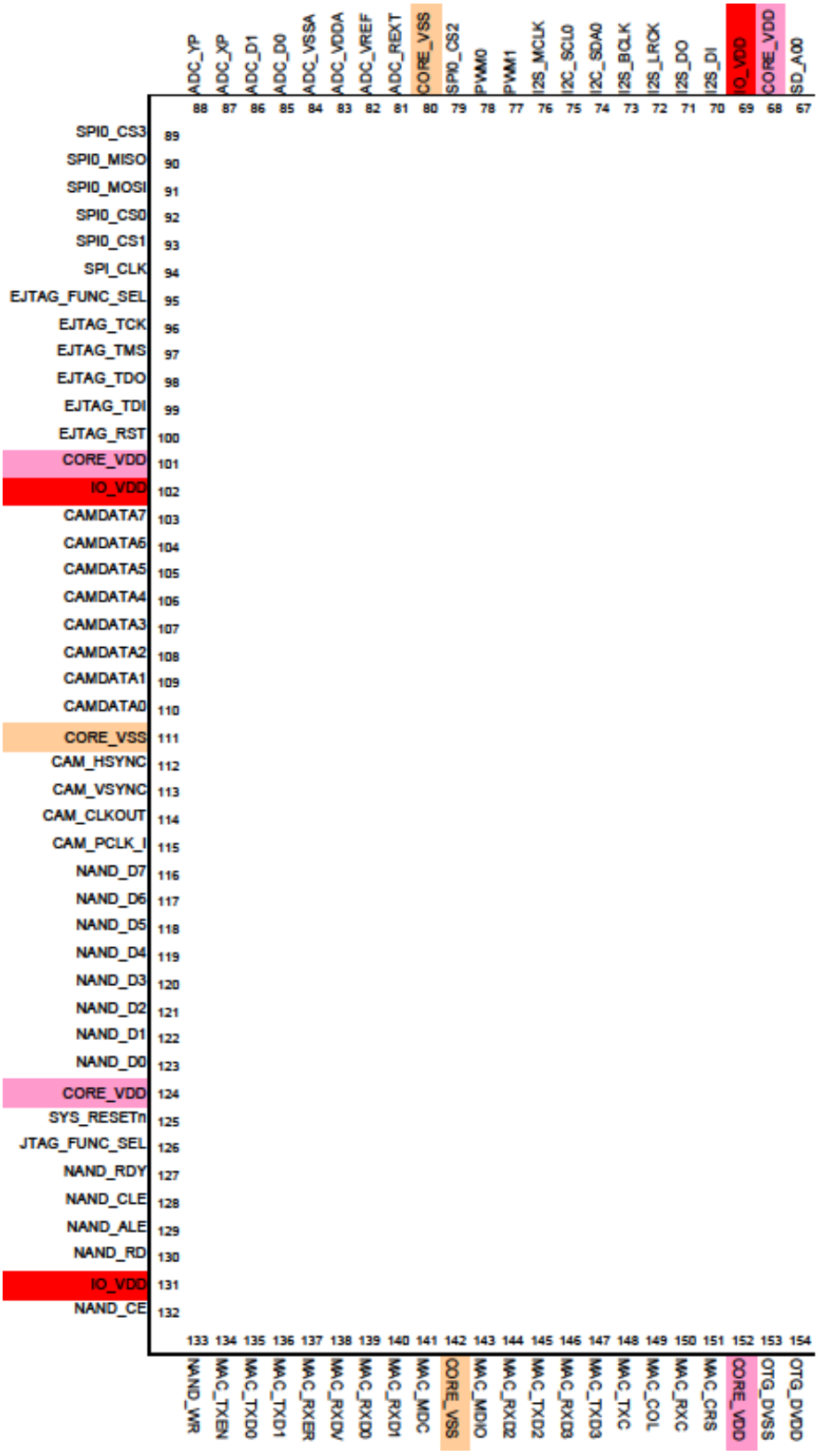


Figure 6-2 QFP176A pin permutation (left figure)

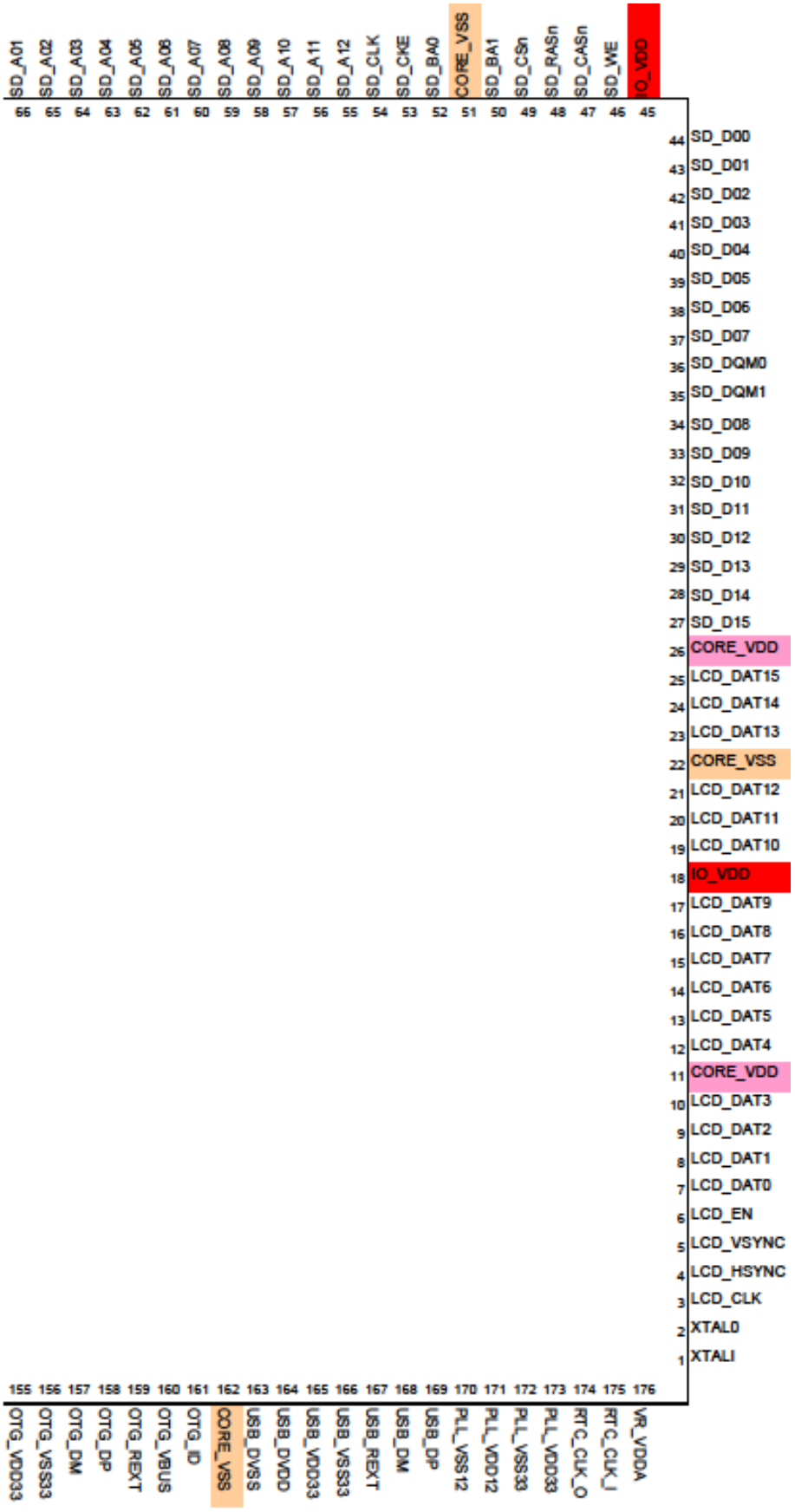


Figure 6-3 QFP176A top pin permutation (right figure)

6.2.3 QFP176U top pin permutation

QFP176U top pin permutation is shown in Figure 6-4 and 6-5.

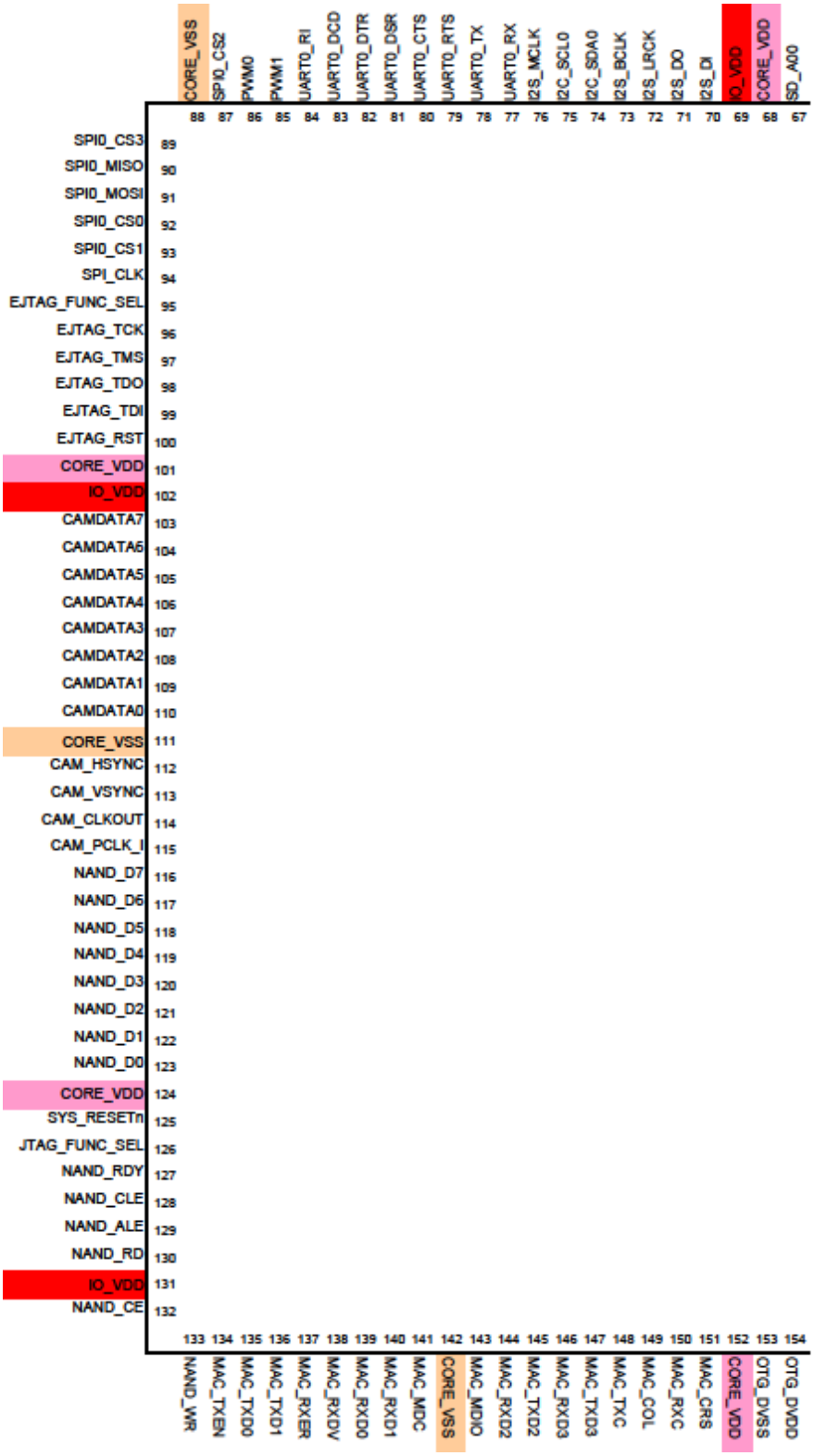


Figure 6-4 QFP176U pin permutation (left figure)

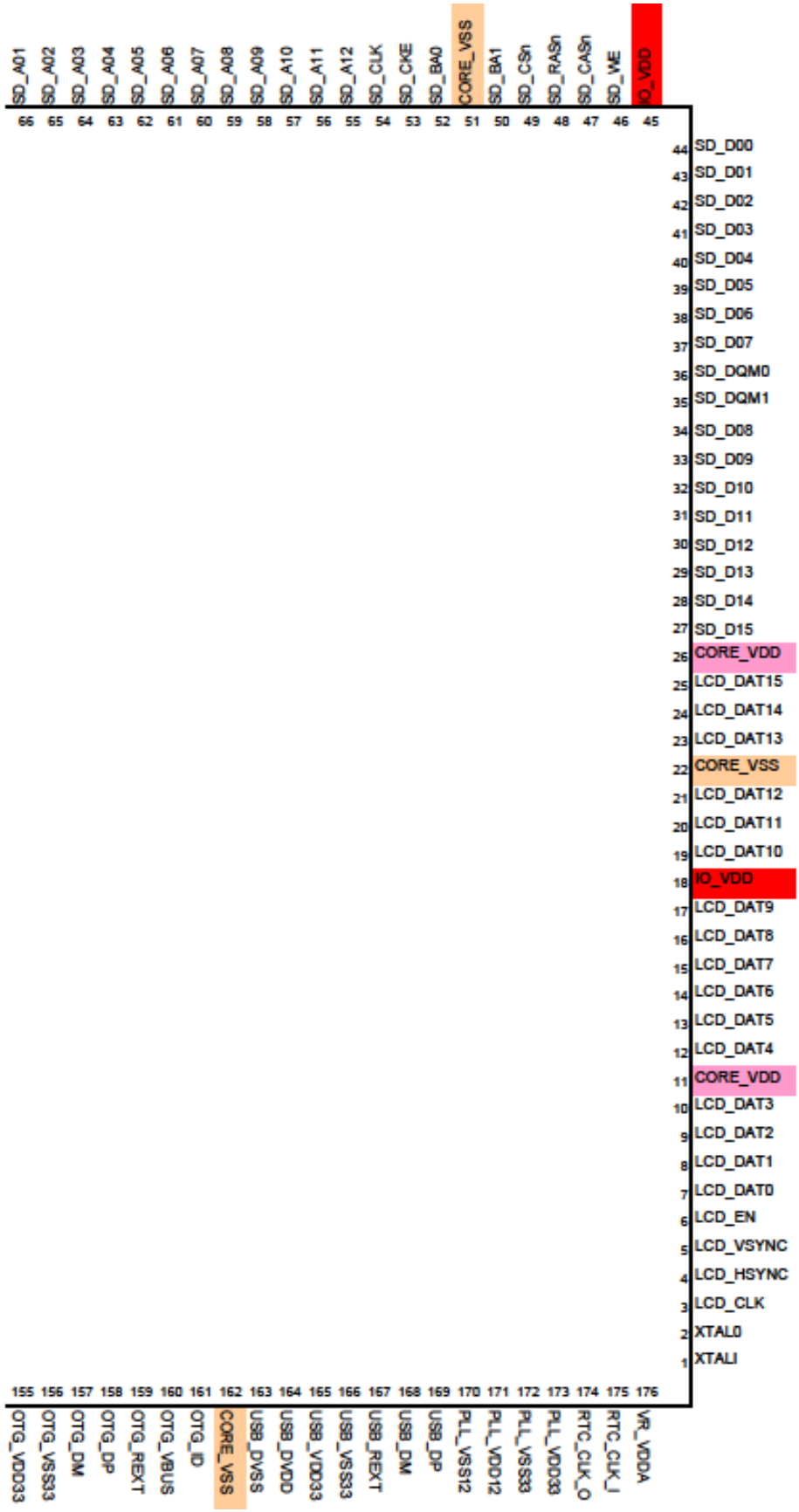
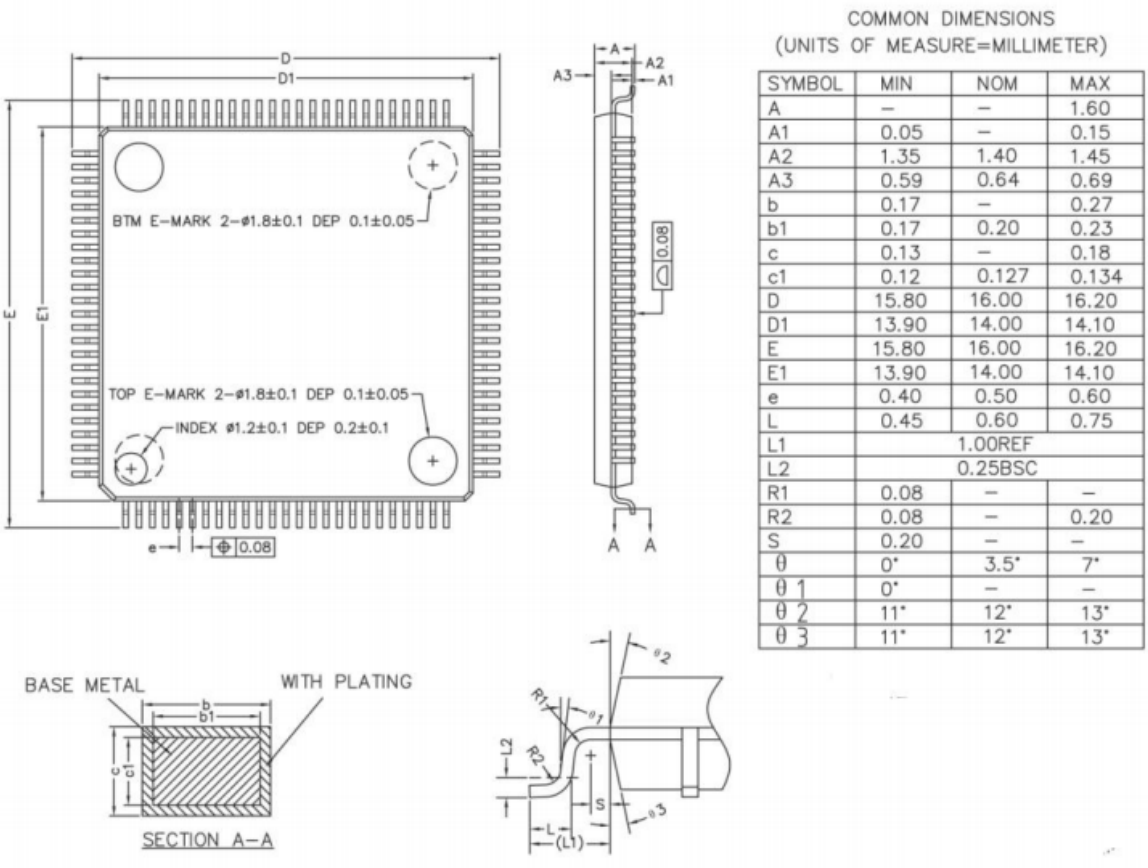


Figure 6-5 QFP176U top pin permutation (right figure)

7 Package Mechanical Dimensions

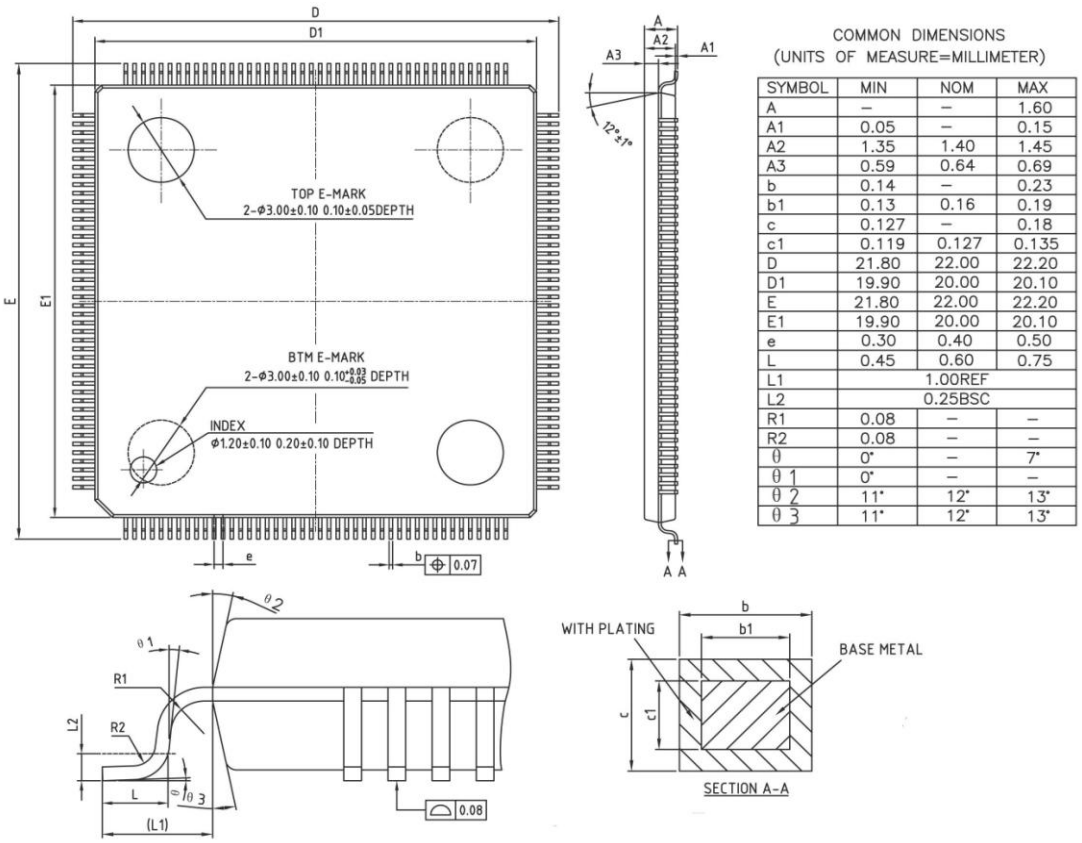
7.1.1 Mechanical dimension of QFP100 package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

7.1.2 Mechanical dimension of QFP176 package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	–	0.23
b1	0.13	0.16	0.19
c	0.127	–	0.18
c1	0.119	0.127	0.135
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.30	0.40	0.50
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	–
θ	0°	–	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

8 Treatment of Unused Pin

Unused pin needs to be treated under the following principles:

Signal group	Treatment when unused
USB	Can be floated
Input signal	Needs pulling down, or using the software to configure as GPIO output 0.
Output signal	Can be floated
Initialization signal	Configuration pins must be pulled-up/pulled -down properly.
The clock configuration	must be properly connected
Power ground	must be properly connected

9 Appendix

9.1 Pin Multiplexing

Signal names in the below table is given in the sequence of QFP176 package. In QFP100 package, some pins aren't bonded, and expressed as "-". QFP176 has two packages: QFP176A and QFP176U. The difference between two packages is in the 81-88 pins. Therein, QFP176A has ADC interface, and QFP176U has UART interface. In the table, the pin number with A in behind brackets indicates QFP176A package, and that with U in behind brackets QFP176U package.
In addition, some signals of multiplexing signals in table is multiplexed by group. For example, SDRAM/SRAM, SPI0/SDIO, SPI1/SDIO and I2S/AC97, these signals are configured by misc register, and the two signals are divided by "/" in the same cell of multiplexing table.
Notes: compared with 1C1, the 1C2 mainly changes in pin multiplexing. The newly added multiplexing relationship includes UART5-UART11 and SDRAM_CS1 pins, and is distributed in the 4^{th} and 5^{th} multiplexing (see the green part in the table below); in addition, 1C2 transfers the multiplexing relationship of pins LCD_CLK and LCD_EN in 1C1 to LCD_HSYNC and LCD_VSYNC. Namely, in QFP176 package, the multiplexing of pin 3 is transferred to pin 1, and that of pin 6 is transferred to pin 5 (see the yellow part in table 9-1) Table 9-2 shows the multiplexing relationship of pins 3-6 in 1C1 corresponding to the yellow part in table 9-1.

Notes: the default multiplexing relation of the pin is in the last column. Except several pins are used as GPIO, others are all pin definition function; if there is no special instruction in the last column, the multiplexing relation is its pin definition function by default.

The pin multiplexing relation in 1C different packages is shown in the table below.

Table 9-1 Multiplexing relationship table of pin

NAME	PIN_NO QFP176	PIN_NO QFP100	GPIO	The first multiplexing	The second multiplexing	The third multiplexing	The fourth multiplexing	The fifth multiplexing	Default multiplexing
BANK0									
XTALI	1	1							
XTAL0	2	2							
LCD_CLK PIX_CLK	3	3	GPIO76						
LCD_HSYNC	4	-	GPIO74	SPI0_CS1/ Sdio_Dat2	UART0_RX	PWM2	I2C_SDA1	SDRAM_CS1	
LCD_VSYNC	5	-	GPIO75	SPI0_CS2/ Sdio_Dat3	UART0_TX	PWM3	I2C_SCL1		
LCD_EN	6	4	GPIO77						
LCD_D0 LCD_B3	7	-	GPIO58					UART4_RX/ UART0_CTS	
LCD_D1 LCD_B4	8	-	GPIO59					UART4_TX/ UART0_RTS	
LCD_D2 LCD_B5	9	-	GPIO60					UART5_RX/ UART0_DSR	
LCD_D3 LCD_B6	10	-	GPIO61					UART5_TX/ UART0_DTR	
CORE_VDD	11	-							
LCD_D4 LCD_B7	12	-	GPIO62					UART6_RX/ UART0_DCD	
LCD_D5 LCD_G2	13	-	GPIO63					UART6_TX/ UART0_RI	
LCD_D6 LCD_G3	14	-	GPIO64					UART7_RX	
LCD_D7	15	-	GPIO65					UART7_TX	

LCD_G4									
LCD_D8 LCD_G5	16	-	GPIO66					UART8_RX	
LCD_D9 LCD_G6	17	-	GPIO67					UART8_TX	
IO_VDD	18	10							
LCD_D10 LCD_G7	19	-	GPIO68					UART9_RX/ UART8_CTS	
LCD_R3 LCD_D11	20	-	GPIO69					UART9_TX/ UART8_RTS	
LCD_D12 LCD_R4	21	-	GPIO70					UART10_RX/ UART8_DSR	
CORE_VSS	22	14							
LCD_D13 LCD_R5	23	-	GPIO71					UART10_TX/ UART8_DTR	
LCD_D14 LCD_R6	24	-	GPIO72					UART11_RX/ UART8_DCD	
LCD_D15 LCD_R7	25	-	GPIO73					UART11_TX/ UART8_RI	
CORE_VDD	26	16							
SD_D15/ SRAM_D15	27	5	GPIO104	I2C_SCL	PWM3	UART2_TX	MDIO		
SD_D14/ SRAM_D14	28	6	GPIO103	I2C_SDA	PWM2	UART2_RX	MDC		
SD_D13/ SRAM_D13	29	7	GPIO102	UART1_TX	NAND_CE#	I2C_SCL1	PWM1		
SD_D12/	30	8	GPIO101	UART1_RX	NAND_RDY	I2C_SDA1	PWM0		
SRAM_D13									
SD_D11/ SRAM_D11	31	9	GPIO100	I2S_LRCK	NAND_WR#	UART0_TX	CAN1_TX		
SD_D10/ SRAM_D10	32	11	GPIO99	I2S_DI	NAND_ALE	UART0_RX	CAN1_RX		
SD_D09/	33	12	GPIO98	I2S_BCLK	NAND_RD#	I2C_SCL2	CANO_TX		

SRAM_D09									
SD_D08/ SRAM_D08	34	13	GPIO97	I2S_MCLK	NAND_CLE	I2C_SDA2	CAN0_RX		
SD_DQM1/ SRAM_BHEn	35	15	GPIO96	I2S_DO	PWM1	XTALI		UART6_RX/ UART0_DCD	
SD_DQM0/ SRAM_BLEn	36	17							
SD_D07/ SRAM_D07	37	18							
SD_D06/ SRAM_D06	38	19							
SD_D05/ SRAM_D05	39	20							
SD_D04/ SRAM_D04	40	21							
SD_D03/ SRAM_D03	41	22							
SD_D02/ SRAM_D02	42	23							
SD_D01/ SRAM_D01	43	24							
SD_D00/	44	25							
SRAM_D00									
BANK1									
IO_VDD	45	-							
SD_WEn/ SRAM_WEn	46	26							
SD_CASn/ SRAM_A15	47	27							
SD_RASn/ SRAM_A14	48	28							
SD_CSn/ SRAM_CSn	49	29							

SD_BA1/ SRAM_A16	50	30							
CORE_VSS	51	31							
SD_BA0/ SRAM_A17	52	32							
SD_CKE/ SRAM_A13	53	33							
SD_CLK/ SRAM_OEn	54	34							
SD_A12/ SRAM_A12	55	35							
SD_A11/ SRAM_A11	56	36							
SD_A10/ SRAM_A10	57	37							
SD_A09/ SRAM_A09	58	38							
SD_A08/ SRAM_A08	59	39							
SD_A07/ SRAM_A07	60	42							
SD_A06/ SRAM_A06	61	43							
SD_A05/ SRAM_A05	62	44							
SD_A04/ SRAM_A04	63	45							
SD_A03/ SRAM_A03	64	46							
SD_A02/ SRAM_A02	65	47							
SD_A01/ SRAM_A01	66	48							

SD_A00/ SRAM_A00	67	49							
CORE_VDD	68	40							
IO_VDD	69	41							
I2S_DI	70	-	GPIO87					UART7_RX	
I2S_DO	71	-	GPIO88					UART7_TX	
I2S_LRCK	72	-	GPIO89					UART8_RX	
I2S_BCLK	73	-	GPIO90					UART8_TX	
I2C_SDA0	74	-	GPIO85					UART9_RX/ UART8_CTS	
I2C_SCL0	75	-	GPIO86					UART9_TX/	
								UART8_RTS	
I2S_MCLK	76	-	GPIO91						
URT0_RX	77(U)	-	GPIO38						
URT0_TX	78(U)	-	GPIO39						
URT0_RTS	79(U)	-	GPIO41	SRAM_A19	UART1_TX	PWM3	NAND_RDY3		
URT0_CTS	80(U)	-	GPIO40	SRAM_A18	UART1_RX	PWM2	NAND_CE#3		
URT0_DSR	81(U)	-	GPIO42	SRAM_A20	UART2_RX	CAN0_RX	I2C_SDA1		
URT0_DTR	82(U)	-	GPIO43	SRAM_A21	UART2_TX	CAN0_TX	I2C_SCL1		
URT0_DCD	83(U)	-	GPIO44	SRAM_A22	UART3_RX	CAN1_RX	I2C_SDA2		
URT0_RI	84(U)	-	GPIO45	SRAM_A23	UART3_TX	CAN1_TX	I2C_SCL2		
PWM1	77(A) 85(U)	-	GPIO92						
PWM0	78(A) 86(U)	-	GPIO06	CAMCLKOUT					
SPI0_CS2	79(A)	-	GPIO83	Sdio_Dat3					
CORE_VSS	80(A) 88(U)	50							
ADC_REXT	81(A)	-							
ADC_VREF	82(A)	-							
ADC_VDDA	83(A)	-							
ADC_VSSA	84A)	-							

ADC_D0	85(A)	-							
ADC_D1	86(A)	-							
ADC_XP	87(A)	-							
ADC_YP	88(A)	-							

BANK2									
SPI0_CS3	89	-	GPIO84	CAMCLKOUT				UART10_RX/ UART8_DSR	
SPI0_MISO	90	51	GPIO80	Sdio_Cmd				UART4_RX/ UART0_CTS	
SPI0_MOSI	91	52	GPIO79	Sdio_Dat0				UART4_TX/ UART0_RTS	
SPI0_CS0	92	53	GPIO81	Sdio_Dat1			SDRAM_CS1	UART5_RX/ UART0_DSR	
SPI0_CS1	93	-	GPIO82	Sdio_Dat2				UART10_TX/ UART8_DTR	
SPI_CLK	94	54	GPIO78	Sdio_clk				UART5_TX/ UART0_DTR	
EJTAG_SEL	95	55	GPIO00	CAMCLKOUT	I2C_SDA0	CAN0_X	UART3_RX	SDRAM_CS1	GPIO
EJTAG_TCK	96	56	GPIO01	CAMPCLKIN	I2C_SCL0	CAN0_TX	UART3_TX		GPIO
EJTAG_TMS	97	57	GPIO04	CAMDATA1	I2C_SDA2	PWM0	UART2_RX		GPIO
EJTAG_TDO	98	58	GPIO03	CAMHSYNC	I2C_SCL1	CAN1_TX	UART1_TX		GPIO
EJTAG_TDI	99	59	GPIO02	CAMVSYNC	I2C_SDA1	CAN1_RX	UART1_RX		GPIO
EJTAG_RST	100	60	GPIO05	CAMDATA0	I2C_SCL2	PWM1	UART2_TX		GPIO
CORE_VDD	101	61							
IO_VDD	102	62							
CAMDATA7	103	-	GPIO57		LCD_R2	CAN1_TX	I2C_SCL2	UART7_RX	

CAMDATA6	104	-	GPIO56		LCD_R1	CAN1_RX	I2C_SDA2	UART7_TX	
CAMDATA5	105	-	GPIO55		LCD_R0	CAN0_TX	I2C_SCL1	UART8_RX	
CAMDATA4	106	-	GPIO54		LCD_G1	CAN0_RX	I2C_SDA1	UART8_TX	
CAMDATA3	107	-	GPIO53		LCD_G0	CAMCLKOUT	PWM3	UART9_RX/ UART8_CTS	

CAMDATA2	108	-	GPIO52		LCD_B2	SPI1_CS3	PWM2	UART9_TX/ UART8_RTS	
CAMDATA1	109	-	GPIO51		LCD_B1	SPI1_CS2	I2C_SCL2	UART10_RX/ UART8_DSR	
CAMDATA0	110	-	GPIO50		LCD_B0	SPI1_CS1	I2C_SDA2	UART10_TX/ UART8_DTR	
CORE_VSS	111	63							
CAMHSYNC	112	-	GPIO49		NAND_RDY3	SPI1_CS0	I2C_SCL1	UART11_RX/ UART8_DCD	
CAMVSYNC	113	-	GPIO48		NAND_CE#3	SPI1_MOSI	I2C_SDA1	UART11_TX/ UART8_RI	
CAMCLKOUT	114	-	GPIO47	SRAM_A25	NAND_RDY2	SPI1_MISO	PWM3	UART6_RX/ UART0_DCD	
CAMPCLKIN	115	-	GPIO46	SRAM_A24	NAND_CE#2	SPI1_CLK	PWM2	UART6_TX/ UART0_RI	
NAND_7	116	64	GPIO20	SPI1_CS1/ Sdio_Dat2	MAC_MDIO	CAMDATA0	I2C_SCL2		
NAND_6	117	65	GPIO19	SPI1_CS2/ Sdio_Dat3	MAC_MDC	CAMDATA1	I2C_SDA2		
NAND_5	118	66	GPIO18	UART1_TX	UART3_TX	CAMDATA2	PWM2		
NAND_4	119	67	GPIO17	UART1_RX	UART3_RX	CAMDATA3	PWM3		
NAND_3	120	68	GPIO16	SPI1_CS0/ Sdio_Dat1	CAN1_TX	CAMDATA4	I2S_LRCK		

NAND_2	121	69	GPIO15	SPI1_MOSI/ Sdio_Dat0	CAN1_RX	CAMDATA5	I2S_DO		
NAND_1	122	70	GPIO14	SPI1_MISO/ Sdio_Cmd	CAN0_TX	CAMDATA6	I2S_BCLK		
NAND_0	123	71	GPIO13	SPI1_CLK/ Sdio_clk	CAN0_RX	CAMDATA7	I2S_MCLK		GPIO
CORE_VDD	124	72							
SYS_RST_	125	73							
JTAG_SEL	126	74					SDRAM_CS1	UART6_TX/ UART0_RI	
NAND_RDY	127	-	GPIO07						
NAND_CLE	128	-	GPIO08						GPIO
NAND_ALE	129	-	GPIO09						GPIO
NAND_RD#	130	-	GPIO10						GPIO
IO_VDD	131	75							
NAND_CE#	132	-	GPIO11						GPIO
BANK3									
NAND_WR#	133	-	GPIO12						GPIO
MAC_TXCTL	134	76	GPIO21	I2S_MCLK	NAND_CLE	I2C_SDA2	CAN0_RX	UART8_RX	
MAC_TXD0	135	77	GPIO23	I2S_DO	NAND_ALE	UART0_RX	CAN1_RX	UART4_RX/ UART0_CTS	
MAC_TXD1	136	78	GPIO24	I2S_LRCK	NAND_WR#	UART0_TX	CAN1_TX	UART4_TX/ UART0_RTS	
MAC_RXER	137	79	GPIO25	I2S_DI	NAND_RDY0	I2C_SDA1	CAMCLKOUT	UART5_RX/ UART0_DSR	
MAC_RX_DV	138	80	GPIO26	SPI1_CS3	NAND_CE#0	I2C_SCL1	CAMPCLKIN	UART5_TX/ UART0_DTR	GPIO
MAC_RXD0	139	81	GPIO27	I2C_SDA	PWM2	UART2_RX	CAMVSYNC	UART6_RX/ UART0_DCD	GPIO
MAC_RXD1	140	82	GPIO28	I2C_SCL	PWM3	UART2_TX	CAMHSYNC	UART6_TX/	GPIO

								UART0_RI	
MAC_MDC	141	-	GPIO29	CAMDATA7	NAND_CE#1	PWM2	I2C_SCL1	UART8_TX	GPIO
CORE_VSS	142	-							
MAC_MDIO	143	-	GPIO30	CAMDATA6	NAND_RDY1	LCD_B0	I2C_SDA1		GPIO
MAC_RXD2	144	-	GPIO31	CAMDATA5	NAND_CS#2	LCD_B1	CAN1_RX	UART11_RX/ UART8_DCD	GPIO
MAC_TXD2	145	-	GPIO32	CAMDATA4	NAND_RDY2	LCD_B2	CAN1_TX	UART11_TX/ UART8_RI	
MAC_RXD3	146	-	GPIO33	CAMDATA3	UART3_RX	LCD_G0	SPI1_CLK/ Sdio_clk		
MAC_TXD3	147	-	GPIO34	CAMDATA2	UART3_TX	LCD_G1	SPI1_MISO/ Sdio_Cmd		
MAC_TXC	148	83	GPIO22	I2S_BCLK	NAND_RD#	I2C_SCL2	CANO_TX	SDRAM_CS1	
MAC_COL	149	-	GPIO36	CAMDATA0	UART2_RX	LCD_R1	SPI1_CS0/ Sdio_Dat1		
MAC_RXC	150	-	GPIO37	PWM3	UART2_TX	LCD_R2	SPI1_CS1/ Sdio_Dat2		
MAC_CRS (ONLY_MII)	151	-	GPIO35	CAMDATA1	PWM1	LCD_R0	SPI1_MOSI/ Sdio_Dat0		
CORE_VDD	152	-							
OTG_DVSS	153	84							
OTG_DVDD	154	85							
OTG_DVDD33	155	86							
OTG_DVSS33	156	87							
OTG_DM	157	88							
OTG_DP	158	89							
OTG_REXT	159	90							
OTG_VBUS	160	91							
OTG_ID	161	92							
CORE_VSS	162	93							
USB_DVSS	163	-							

USB_DVDD	164	-							
USB_DVDD33	165	-							
USB_DVSS33	166	-							
USB_REXT	167	-							
HOST_DM	168	-							
HOST_DP	169	-							
PLL_VSS12	170	94							
PLL_VDD12	171	95							
PLL_VSS33	172	96							
PLL_VDD33	173	97							
RTC_CLK_O	174	98							
RTC_CLK_I	175	99							
RTC_VR_VDDA	176	100							

Table 9-2 1 Multiplexing relationship table of 1C1 pin 3-6

NAME	PIN_NO QFP176	PIN_NO QFP100	GPIO	The first multiplexing	The second multiplexing	The third multiplexing	The fourth multiplexing	The fifth multiplexing
LCD_CLK PIX_CLK	3	3	GPIO76	SPI0_CS1/ Sdio_Dat2	UART0_RX	PWM2	I2C_SDA1	
LCD_HSYNC	4	-	GPIO74					
LCD_VSYNC	5	-	GPIO75					
LCD_EN	6	4	GPIO77	SPI0_CS2/ Sdio_Dat3	UART0_TX	PWM3	I2C_SCL1	