Loongson 1C300 Processor User Manual

Version 1.0

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Loongson Technology Corporation Limited

Reading Guide

Loongson 1C300 Processor User's Manual mainly introduces the architecture and register of Loongson 1C300. For more information about LS232 high-performance processor core integrated by Loongson 1C300, please refer to *Loongson LS232 Processor User Manual*. Loongson 1C300 is hereinafter referred to as Loongson 1C.

Revision history

Date	Edit	Version	Change
Mar. 14, 2013	R&D Centre	0.0.1	First draft
Jun. 16, 2013	R&D Centre	0.0.2	
Mar. 29, 2013	R&D Centre	0.0.3	Supplement the description of DWT and interrupt configuration register; revise the description of modules such as CAMIF, UART and OTG.
Apr. 15, 2013	R&D Centre	0.1	Address space revision
Apr. 26, 2013	R&D Centre	0.2	
Feb. 12, 2014	R&D Centre	0.3	Modify and typeset
Feb. 28, 2014	R&D Centre	0.9	Modify 1C2 changes after revision
Apr. 21, 2014	R&D Centre	1.0	Add the descriptions on pull-up/pull-down in the pin Add the description of SRAM pin and revise some errors. Chip name is updated as Loongson 1C 300

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1 Overview

Loongson 1C chip is a cost-effective single chip system based on LS232 processor core, and is applicable to fields such as biological recognition of fingerprints and Internet of Things sensing.
1C includes the floating point processing unit, and can effectively enhance the processing ability of system floating point data. The memory interface of 1C supports several types of memories and allows the flexible system design. It supports 8-bit SLC NAND or MLC NAND FLASH, and provides the storage expansion interface of high capacity.
1C has provided various serial peripheral interfaces and on-chip modules for developers, including Camera controller, USB OTG 2.0 and USB HOST 2.0 interfaces, AC97/I2S controller, LCD controller, ADC controller, high-speed SPI interface, full-function UART interface, and owns the sufficient computing ability and multi-application connecting ability. It integrates RTC function, and is used to maintain the real time clock.

1.1 System Architecture Chart

Hierarchical bus architecture is adopted inside Loongson 1C. Processor core, memory controller, graphic display controller, CAMERA interface module and AXI_MUX are interconnected by crossbar OTG, MAC, USB and DMA controllers and SPI are connected to crossbar via AXI_MUX. Low-speed peripherals (I2C, I2S, PWM, UART, etc.) are connected to crossbar via AXI2APB.

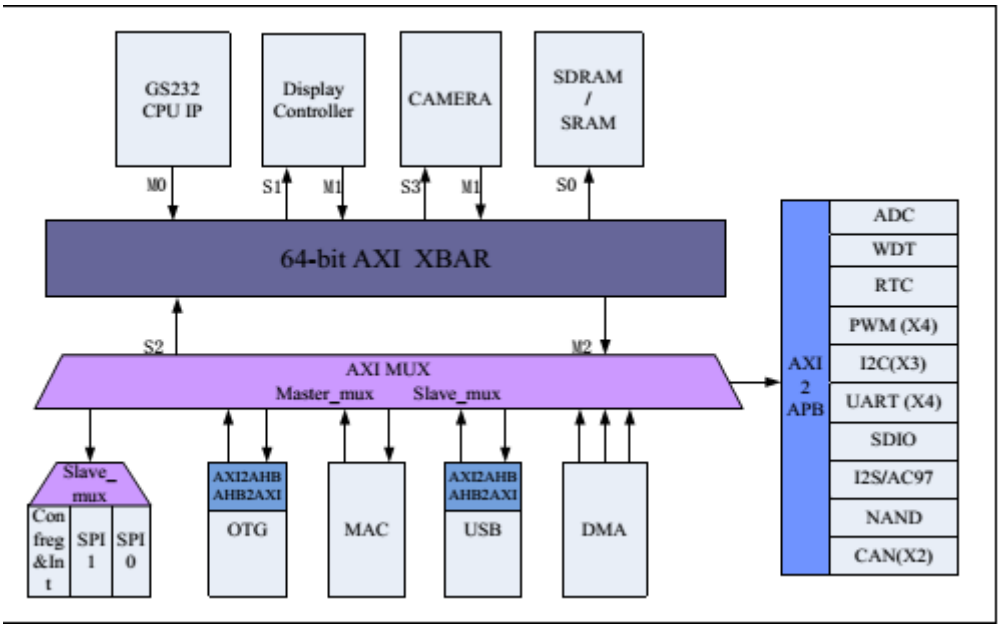

Figure 1-1 Architecture chart of Loongson 1C

1.2 Main Functions of the Chip

1.2.1 Processor core

- Instruction sets of single core LS232 and MIPS32 are compatible, and the dominant frequency is 300MHZ.
- It supports the highly effective dual-issue technology (one clock tick performs two instructions)
- It supports the out-of-order issue and execution technologies such as register renaming, dynamic scheduling, and branch prediction
- 5-stage pipeline(instruction fetch, coding, issue, execution, write back and submit) microarchitecture
- 16KB data cache and 16KB instruction cache
- It integrates 64bit floating point processing unit, supports the fully pipelining of 64bit floating point additive and multiplying operation. Its hardware has accomplished the floating point division operation.

1.2.2 SDRAM Controller

- SDRAM operation, operating frequency of 45~133MHz
- It supports the bus width of 8/16bit parallel data.
- It supports the auto-refresh and self-refresh functions, and page mode.

1.2.3 SRAM/NOR FLASH Controller

- SRAM and NOR Flash direct link interface, working frequency of 66~133MHz
- It supports the chip select pin of static memory, and can be configured separately.
- It supports the bus width of 8bit/16bit parallel data.

1.2.4 NAND Controller

- It supports the single capacity of 4GB NAND FLASH at most
- It supports the FLASH of 512 bytes, 2K byte page, 4K byte page and 8K byte page.
- Hardware ECC generation, detection and indication (software error correction)
- It supports the data reading speed of 8~10MB/S and writing speed of 5MB/s from Flash
- It supports the boot from NAND Flash
- Support mode of little endian

1.2.5 Clock generator

- It has one standard PLL input interface, and supports the external crystal as chip clock input.
- It supports the on-chip output and can configure one way of clock for off-chip peripherals.
- PLL configurable frequency software

1.2.6 I^2S controller

- It supports I^2S input in master mode
- It supports I^2S output in master mode
- It supports the width of 8, 16, 18, 20, 24 and 32 bits.
- It supports audio data of mono and stereo
- It supports the sampling frequency of (16, 22.05, 32, 44.1 and 48) kHz
- It supports DMA transmission mode

1.2.7 AC97 controller

- Variable sampling rate AC97 coder and decoder interfaces (48KHz and below)
- It supports the stereo PCM and single-track MIC input
- It supports 2-channel stereo PCM output
- It support DMA and interrupt operation
- It supports 16, 18 and 20bits sampling precision, and variable sampling rate.
- It supports 16bits, and 16 entry FIFOs for each channel.

1.2.8 LCD controller

- It support 16/24-bit pixel mode
- It supports the display output of RGB444/555/565/888
- It supports the pixel of 1024x768, 800x600, 640-x480 and 320-x240
- It supports DMA transmission mode

1.2.9 Camera interface

- It supports ITU-R BT.601/656 8bit input.
- It supports RAW RGB, RGB565 and YUV4:2:2 data input.
- It supports YUV, RGB888, RGB0888 and RGB565 outputs

- It supports the pixel zooming of 320x240 and 640x480
- It supports the pixel input of 2Kx2K at most, and the pixel can be configured.
- It supports DMA transmission mode

1.2.10 MAC controller

- It supports 10/100Mbps PHY device, including 10 Base-T, 100 Base-TX, 100Base-FX and 100 Base-T4;
- It's completely compatible with IEEE standard 802.3
- It's completely compatible with 802.3x full duplex flow control and half-duplex back pressure flow control
- It supports VLAN frames
- It supports DMA transmission mode
- It supports standard media independent interface (MII)
- It supports the standard simplified MII interface (RMII), and may connect the external PHY chip.

1.2.11 USB2.0 controller

- One USB OTG2.0 controller
- One USB HOST2.0 controller
- It supports high-speed and full-speed mode
- It supports DMA transmission mode
- It's compatible with USB Rev 1.1 and USB Rev 2.0 protocols

1.2.12 SPI controller

- It supports two-way independent SPI interface, and each way of SPI interface supports four chip selects.
- Follow specifications of serial peripheral interface (SPI)
- It supports synchronous, serial and full duplex communication
- It supports SPI master mode
- 8-bit in per transmission
- It supports inquiries and interrupt transmission mode
- It supports the SPI nor flash boot.
- It supports SPI interface two-way input and output, and the maximum data transmission speed is 24~96 Mbps.
- It supports the minimum communication rate as low as 25KB, and facilitates the matching of special device.

1.2.13 I^2C controller

- Three-channel standard I^2C bus interface
- It supports configuration of master, slave or master / slave mode
- Programmable bus clock frequency

1.2.14 UART controller

- It supports two full-function serial ports. Therein, the full-function serial port 0 can multiplex four two-wire serial interfaces or two four-wire serial interfaces, and supports the smart card protocol.
- RxD0, TxD0, RxD1, TxD1, RxD2 and TxD2 based on interrupt operation;
- UART channel 0, 1 and 2 with IrDA 1.0
- UART channel 0 and 1 with RTS0, CTS0, RTS1 and CTS1

1.2.15 GPIO

- It supports 105 GPIO at most
- All GPIO (except boot and system configuration) is defaulted as input after reset
- All GPIO support interrupt function
- Each GPIO pin supports the level-triggered and edge-triggered modes, and can be configured independently.
- GPIO base pin rate up to 4MHz

1.2.16 PWM controller

- Four-way 32bits can configure PWM timer.
- It supports timer function
- It supports counter function

1.2.17 RTC

- Timing is accurate to 0.1 second
- It supports the external crystal as RTC clock input.
- It supports the operation powered by external battery, and later by battery after powered off.
- The special power pin may be connected to the battery or 3.3V main power supply.
- Provide seconds, minutes, hours, days, months and years

1.2.18 CAN controller

2-channel independent CAN controller

- It's compatible with CAN2.0A and CAN2.0B protocols (the passive expansion frame in PCA82C200 compatible mode)
- It supports CAN protocol extensions
- Bit rate up to 1Mbits / s

1.2.19 SDIO controller

- channel independent CAN controller
- It's compatible with SD Memory 2.0/MMC/SDIO 2.0 protocol.
- It supports SDIO start

1.2.20 ADC controller

- Sampling rate up to 1MHz at most
- 4-channel ADC input
- It supports 4-wire and 5-wire touch screens
- It supports continuous sampling and single sampling
- It supports analog watchdog

2 Definition of Pin

2.1 Conventions

The instructions of Loongson 1C pin in this chapter use the following protocols:
The input and output types of signals are represented by code. See Table 2-1.

Table 2-1 Signal Type Code

Code	Description
A	Simulation
DIFF I/O	Two-way difference
DIFF IN	Difference input
DIFF OUT	Difference output
I	Input.
I/O	Bidirectional
0	Output
OD	Open-drain output
P	Power supply
G	Ground

2.2 LCD Interface

Signal name	Type	Pull-up/pull-down	Description
LCD_CLK	O	PU	LCD clock signal
LCD_HSYNC	O	PU	LCD horizontal synchronizing signal
LCD_VSYNC	O	PU	LCD vertical synchronizing signal
LCD_EN	O	PU	LCD enable signal
LCD_DAT[15:0]	O	PU	LCD data signal

[Notes] In QFP100 package, LCD interface can't be used. In QFP176 encapsulation, LCD may use 16bit and 24bit mode. In 16bit mode, the pin won't be multiplexed; in 24bit mode, the low bit needs to multiplex CAM_DAT [7:0] or MAC signal.

2.3 SDRAM Interface

Signal name	Type	Pull-up/ pull-down	Description
SD_CLK	O	-	SDRAM clock signal
SD_CKE	O	-	SDRAM clock enable signal
SD_CSn	O	-	SDRAM chip selection signal, active low
SD_RASn	O	-	SDRAM line gating signal, effective low level
SD_CASn	O	-	SDRAM column selection signal, active low
SD_WE	O	-	SDRAM read-write signal, writing as low level
SD_BA[1:0]	O	-	Bank signal of SDRAM, four banks in total
SD_ADDR[12:0]	O	-	SDRAM address signal
SD_DATA[15:0]	I/O	-	SDRAM data signal
SD_DQM[1:0]	O		SDRAM data mask signal

2.4 SRAM/NOR Flash Interface

Signal name	Type	Pull-up/ pull-down	Description
SRAM_CSn	O	-	SRAM chip selection signal, active low
SRAM_WEn	O	-	SRAM writing enable signal, active low
SRAM_OEn	O	-	SRAM reading enable signal, active low
SRAM_OEn	O	-	SRAM reading enable signal, active low
SRAM_DATA[15:0]	I/O	-	SRAM data signal
SRAM_BHE	O		SRAM high Byte Data desired signal
SRAM_BLE	O		SRAM low Byte Data effective signal

2.5 I2S Interface

Signal name	Type	Pull-up/ pull-down	Description
I2S_MCLK	O	PU	I2S clock signal
I2S_BCLK	O	PU	I2S bit clock signal
I2S_LRCK	O	PU	I2S channel selection signal
I2S_DI	I	PU	I2S data serial input signal
I2S_DO	O	PU	I2S data serial output signal

[Notes] In QFP100 package, I2S interface isn't introduced, and needs to be multiplexed with MAC pin. In QFP176 package, I2S interface is introduced, and can be directly used.

2.6 I 2C Interface

Signal name	Type	Pull-up/ pull-down	Description
I2C[2:0]_SCL	O	No elicitation	I^2C serial clock
I2C[2:0]_SDA	I/O	No elicitation	I^2C serial data

[Notes] In QFP100 and QFP176 packages, I2C interface isn't introduced, and needs to be multiplexed with MAC, EJTAG, LCD or CAM pin.

2.7 UART Interface

Signal name	Type	Pull-up/ pull-down	Description
UART0_TX	O	PU	UART0 data transmission
UART0_RX	I	PU	UART0 data reception
UART0_RTS	I	PU	UART0 reception request
UART0_CTS	I	PU	UART0 reception permission
UART0_DSR	I	PU	UART0 device ready
UART0_DTR	O	PU	UART0 data terminal ready
UART0_DCD	I	PU	UART0 carrier detection
UART0_RI	I	PU	UART0 ringing tips

[Notes] In QFP100 package, there is no full-function serial interface, and only two-wire type. In QFP176D

package, the full-function serial interface can be directly used.

2.8 PWM Interface

Signal name	Type	Pull-up/ pull-down	Description
PWM0	O	PU	PWMO impulse output
PWM1	O	PU	PWM1 impulse output
PWM2	O	No elicitation	PWM2 impulse output
PWM3	O	No elicitation	PWM3 impulse output

[Notes] In QFP100 package, PWM isn't introduced and needs to be multiplexed with others. In QFP176 package, PWM0 and PWM1 can be directly used, and PWM2 and PWM3 need to be multiplexed with others.

2.9 ADC Interface

Signal name	Type	Pull-up/ pull-down	Description
ADC_REXT	I	-	ADC reference resistor
ADC_VREF	I	-	ADC reference voltage
ADC_VDDA	I	-	ADC analog power supply
ADC_VSSA	I	-	ADC analog ground
ADC_D0	I	-	ADC Channel Zero sampling input
ADC_D1	I	-	ADC Channel 1 sampling input
ADC_XP	I	-	The 2nd channel sampling input of touch screen X+/ADC
ADC_YP	I	-	The 3rd channel sampling input of touch screen X+/ADC

[Notes] The AD interface can only be used In QFP176A package.

2.10 SPI Interface

Signal name	Type	Pull-up/ pull-down	Description
SPI_SCK	O	PU	SPI clock output
SPI[3:0]_CSn	O	PU	SPI chip selection 0 to 3
SPI_MOSI	O	PD	SPI data output
SPI_MISO	I	PD	SPI data input

2.11 EJTAG Interface

Signal name	Type	Pull-up/ pull-down	Description
EJTAG_SEL	I	PU	JTAG selection(0: JTAG, 1: EJTAG)
JTAG_SEL	I	PU	JTAG pin function multiplex (when the bit is 1, select the multiplex function)
EJTAG_TCK	I	PU	JTAG clock
EJTAG_TDI	I	PU	JTAG data input
EJTAG_TMS	I	PU	JTAG mode
EJTAG_TRST	I	PU	JTAG reset, to be pull down
EJTAG_TDO	O	PU	JTAG data output

[Notes] EJTAG_SEL select whether is JTAG or EJTAG. JTAG_SEL is used to choose JTAG multiplex function. Please don't be confused.

2.12 CAMERA Interface

Signal name	Type	Pull-up/ pull-down	Description
CAM_CLKOUT	O	PU	Camera reference clock output
CAM_PCLK_I	I	PU	Camera pixel clock input
CAM_HSYNC	I	PU	Camera horizontal synchronization signal
CAM_VSYNC	I	PU	Camera vertical synchronizing signal
CAMDATA[7:0]	I	PU	Camera data input

[Notes] In QFP100 packaging, CAM isn't bounded out and needs to be multiplexed with NAND and MAC. In QFP176 package, CAM can be directly used.

2.13NAND Interface

Signal name	Type	Pull-up/ pull-down	Description
NAND_CLE	O	PD	NAND command latch
NAND_ALE	O	PD	NAND address latch
NAND_RD	O	PD	NAND read signal
NAND_WR	O	PD	NAND write signal
NAND_CE	O	PD	NAND chip selection 0
NAND_RDY	I	PD	NAND ready 0
NAND_D [7:0]	I/O	PD	NAND address / data lines

2.14 MAC Interface

Signal name	Type	Pull-up/ pull-down	Description
MAC_TXCK	O	PU	MII clock transmission
MAC_TXEN	O	PU	MII control transmission
MAC_TXD[3:0]	O	PU	MII data transmission
MAC_RXCK	I	PU	MII clock reception
MAC_RXDV	I	PU	MII control reception
MAC_RXD[3:0]	I	PU	MII data reception
MAC_MDCK	O	PU	SMA interface clock
MAC_MDIO	I/O	PU	SMA interface data
MAC_COL	I	PU	MAC Collision detection
MAC_CRS	I	PU	MAC carrier wave detection

[Notes] In QFP package, MAC can only use RMII mode. In QFP176 package, MII and RMII modes can be used.

2.15 OTG Interface

Signal name	Type	Pull-up/ pull-down	Description
OTG_DVDD			OTG digital power
OTG_DVSS			OTG digital ground
OTG_VDD33			OTG analog power supply
OTG_VSS33			OTG analog ground
OTG_REXT			OTG reference resistor
OTG_DP	DIFF I/O	-	OTG differential signal line D +
OTG_DM	DIFF I/O	-	OTG differential signal line D —
OTG_VBUS			OTG_VBUS
OTG_ID			OTG_ID

2.16 USB Port

Signal name	Type	Pull-up/ pull-down	Description
USB_DVDD			USB digital power
USB_DVSS			USB digital ground
USB_VDD33			USB analog power supply
USB_VSS33			USB analog ground
USB_REXT			USB reference resistor
USB_DP	DIFF I/O	-	USB differential signal line D +
USB_DM	DIFF I/O	-	USB differential signal line D －

[Notes] In QFP100 package, USB HOST can't be used. In QFP176 package, it can be used.

2.17 RTC Interface

Signal name	Type	Pull-up/pull-down	Description
RTC_CLK_I	I	-	RTC oscillator input, connect 32.768K oscillator
RTC_CLK_O	O	-	RTC crystal oscillator output
VR_VDDA			RTC power supply

2.18 Clock Configuration Signal

Signal name	Type	Pull-up/pull-down	Description
XTALI	I	-	System clock crystal oscillator input, connect to 24M
XTAL0	O	-	System clock crystal oscillator output

2.19 Power Ground

Signal name	Type	Pull-up/pull-down	Description
PLL_ VDD33	P		Core PLL analog power supply
PLL_ VSS33	G		Core PLL analog ground
PLL_VDD12	P		Core PLL digital power supply
PLL_VSS12	G		Core PLL digital ground
CORE_VDD	P		Core voltage power supply
CORE_VSS	G		Core voltage ground
IO_VDD	P		IO power supply

2.20 Initialization Signal

Loongson 1C has three starting modes: SPI FLASH, NAND FLASH and SDIO. Multiplex function pin obtains the configuration message from the pull-up and pull-down values during system reset for the software to judge the powered state.

Table 2-1 Configuration signal

Pin name	Signal name	Description
NAND_D [3:0]	start_freq	CPU PLL frequency configuration in hardware control mode The frequency calculation formula shall be:

		Freq = 6*(4*NAND_D[3:0] + 40)
NAND_D [5:4]	boot_sel	Boot selection is different in QFP100 and QFP176 packages (in QFP100 packages, the control signal of NAND isn't bonded to the pin) In QFP100 package, boot_sel is 00: Reserved 01: it indicates the boot from SPI flash 10: it indicates the boot from NAND flash (multiplex SDRAM pin) 11: it indicates the boot from NAND flash (multiplex MAC pin) In QFP176 packaging, boot_sel is 00: Reserved 01: it indicates the boot from SPI flash 10: it indicates the boot from NAND flash 11: it indicates the boot from SDIO
NAND_D [7:6]	nand_type	In NAND boot, configure the capacity of NAND flash 00: it indicates that the capacity is equal to 2Gb (2KB page) 01: it indicates that capacity is 1Gb (2KB page) 10: it indicates that the capacity is 512Mb (512 Bytes page) 11: it indicates the capacity is low and equal to 256MB (512 Bytes page)
NAND_CLE	rs_rd_cfg	In NAND boot, whether to adopt ECC, select NAND only in boot_sel Flash valid at startup When the bit is 0, it indicates the non-ECC boot of NAND When the bit is 1, it indicates the ECC boot of NAND
SPI0_CLK	usb_refclksel	Clock selective signal of USB_HOST and USB_OTG When the bit is 1, it indicates the clock is provided by PLL. When the bit is 0, it indicates the clock is provided by external oscillator.

3 Register Definition

3.1 Base Register Definition

Register name	Address	RW (read/write) (R/W)	Function description	Reset value
Base register				
START_FREQ	0xbfe7_8030	R/W	PLL frequency configuration and SDRAM frequency division factor	Charged state
CLK_DIV_PARAM	0xbfe7_8034	R/W	CPU/CAMERA/DC frequency division factor	0x0
CBUS_CONFSIGNALS	0xbfd0_0400	R/W		0x0
CBUS_SD_CTRL0	0xbfd0_0410	R/W	SDRAM parameter configuration register	0x001438a3
CBUS_SD_CTRL1	0xbfd0_0414	R/W	SDRAM parameter configuration register	0x80000080
SHUT_CTRL	0xbfd0_0420	R/W	Each module switch register	0x0
MISC_CTRL	0xbfd0_0424	R/W	Function multiplexing register 0	0x4
cpu_throt	0xbfe7_c010	R/W	CPU dynamic frequency reduction register	0x0
Interrupt register				
INTISR0	0xbfd0_0140	R	Interrupt status register 0	0x0
INTEN0	0xbfd0_0144	R/W	Interrupt enable register 0	0x0
INTSET0	0xbfd0_0148	R/W	Interrupt setting register 0	0x0
INTCLR0	0xbfd0_014c	R/W	Interrupt clear register 0	0x0
INTPOL0	0xbfd0_0150	R/W	Interrupt triggering level flag register 0	0x0
INTEDGE0	0xbfd0_0154	R/W	Interrupt triggering edge flag register 0	0x0
INTISR1	0xbfd0_0158	R	Interrupt status register 1	0x0
INTEN1	0xbfd0_015c	R/W	Interrupt enable register 1	0x0
INTSET1	0xbfd0_0160	R/W	Interrupt setting register 1	0x0
INTCLR1	0xbfd0_0164	R/W	Interrupt clear register 1	0x0
INTPOL1	0xbfd0_0168	R/W	Interrupt triggering level flag register 1	0x0
INTEDGE1	0xbfd0_016c	R/W	Interrupt triggering edge flag register 1	0x0
INTISR2	0xbfd0_0170	R	Interrupt status register 2	0x0
INTEN2	0xbfd0_0174	R/W	Interrupt enable register 2	0x0
INTSET2	0xbfd0_0178	R/W	Interrupt setting register 2	0x0
INTCLR2	0xbfd0_017c	R/W	Interrupt clear register 2	0x0
INTPOL2	0xbfd0_0180	R/W	Interrupt triggering level flag register 2	0x0
INTEDGE2	0xbfd0_0184	R/W	Interrupt triggering edge flag register 2	0x0
INTISR3	0xbfd0_0188	R	Interrupt status register 3	0x0
INTEN3	0xbfd0_018c	R/W	Interrupt enable register 3	0x0
INTSET3	0xbfd0_0190	R/W	Interrupt setting register 3	0x0
INTCLR3	0xbfd0_0194	R/W	Interrupt clear register 3	0x0
INTPOL3	0xbfd0_0198	R/W	Interrupt triggering level flag register 3	0x0

INTEDGE3	0xbfd0_019c	R/W	Interrupt triggering edge flag register 3	0x0
INTISR4	0xbfd0_01ª0	R	Interrupt status register 4	0x0
INTEN4	0xbfd0_01ª4	R/W	Interrupt enable register 4	0x0
INTSET4	0xbfd0_01ª8	R/W	Interrupt setting register 4	0x0
INTCLR4	0xbfd0_01ac	R/W	Interrupt clear register 4	0x0
INTPOL4	0xbfd0_01b0	R/W	Interrupt triggering level flag register 4	0x0
INTEDGE4	0xbfd0_01b4	R/W	Interrupt triggering edge flag register 4	0x0
–GPIO register				
GPIO_CFG0	0xbfd0_01c0	R/W	GPIO configuration register 0	0xffe00040
GPIO_CFG1	0xbfd0_01c4	R/W	GPIO configuration register 1	0xfc00_3f3f
GPIO_CFG2	0xbfd0_01c8	R/W	GPIO configuration register 2	0x1ff0_3fff
GPIO_CFG3	0xbfd0_01cc	R/W	GPIO configuration register 3	0x0
GPIO_OE0	0xbfd0_01d0	R/W	GPIO output enable register 0	
GPIO_OE1	0xbfd0_01d4	R/W	GPIO output enable register 1	0xfc00_3f3f
GPIO_OE2	0xbfd0_01d8	R/W	GPIO output enable register 2	0x1ff0_3fff
GPIO_OE3	0xbfd0_01dc	R/W	GPIO output enable register 3	0x0
GPIO_IN0	0xbfd0_01e0	R/W	GPIO input register 0	0x0
GPIO_IN1	0xbfd0_01e4	R/W	GPIO input register 1	0x0
GPIO_IN2	0xbfd0_01e8	R/W	GPIO input register 2	0x0
GPIO_IN3	0xbfd0_01ec	R/W	GPIO input register 3	0x0
GPIO_OUT0	0xbfd0_01f0	R/W	GPIO output register 0	0x0
GPIO_OUT1	0xbfd0_01f4	R/W	GPIO output register 1	0x0
GPIO_OUT2	0xbfd0_01f8	R/W	GPIO output register 2	0x0
GPIO_OUT3	0xbfd0_01fc	R/W	GPIO output register 3	0x0
Multiplexed relationship register				
CBUS_FIRST0	0xbfd0_11c0	R/W	First multiplexed register 0	0x0
CBUS_FIRST1	0xbfd0_11c4	R/W	First multiplexed register 1	0x0
CBUS_FIRST2	0xbfd0_11c8	R/W	First multiplexed register 2	0x0
CBUS_FIRST3	0xbfd0_11cc	R/W	First multiplexed register 3	0x0
CBUS_SECOND0	0xbfd0_11d0	R/W	Second multiplexed register 0	0x0
CBUS_SECOND1	0xbfd0_11d4	R/W	Second multiplexed register 1	0x0
CBUS_SECOND2	0xbfd0_11d8	R/W	Second multiplexed register 2	0x0
CBUS_SECOND3	0xbfd0_11dc	R/W	Second multiplexed register 3	0x0
CBUS_THIRD0	0xbfd0_11e0	R/W	Third multiplexed register 0	0x0
CBUS_THIRD1	0xbfd0_11e4	R/W	Third multiplexed register 1	0x0
CBUS_THIRD2	0xbfd0_11e8	R/W	Third multiplexed register 2	0x0
CBUS_THIRD3	0xbfd0_11ec	R/W	Third multiplexed register 3	0x0
CBUS_FOURTH0	0xbfd0_11f0	R/W	Fourth multiplexed register 0	0x0
CBUS_FOURTH1	0xbfd0_11f4	R/W	Fourth multiplexed register 1	0x0
CBUS_FOURTH2	0xbfd0_11f8	R/W	Fourth multiplexed register 2	0x0
CBUS_FOURTH3	0xbfd0_11fc	R/W	Fourth multiplexed register 3	0x0
DMA configuration register				
ORDER_ADDR_IN	0xbfd0_1160	R/W	DMA configuration register	

3.2 Each Module Register Definition

Register name	Address	R/W	Function description	Reset value
SDRAM interface				

SD_CONFIG[31:0]	0xbfd0_0410	R/W	SDRAM parameter configuration register	0x30d0db5a
SD_CONFIG[63:32]	0xbfd0_0414	R/W	SDRAM parameter configuration register	0x50
PWM0				
CNTR	0xbfe5_c000	R/W	Basic counter	0x0
HRC	0xbfe5_c004	R/W	High pulse timing reference register	0x0
LRC	0xbfe5_c008	R/W	Low pulse timing reference register	0x0
CTRL	0xbfe5_c00c	R/W	Control register	0x0
PWM1				
CNTR	0xbfe5_c010	R/W	Basic counter	0x0
HRC	0xbfe5_c014	R/W	High pulse timing reference register	0x0
LRC	0xbfe5_c018	R/W	Low pulse timing reference register	0x0
CTRL	0xbfe5_c01c	R/W	Control register	0x0
PWM2				
CNTR	0xbfe5_c020	R/W	Basic counter	0x0
HRC	0xbfe5_c024	R/W	High pulse timing reference register	0x0
LRC	0xbfe5_c028	R/W	Low pulse timing reference register	0x0
CTRL	0xbfe5_c02c	R/W	Control register	0x0
PWM3				
CNTR	0xbfe5_c030	R/W	Basic counter	0x0
HRC	0xbfe5_c034	R/W	High pulse timing reference register	0x0
LRC	0xbfe5_c038	R/W	Low pulse timing reference register	0x0
CTRL	0xbfe5_c03c	R/W	Control register	0x0
I2S interface				
IISVersion	0xbfe6_0000	R/W	I2S identify register	0x0
IISConfig	0xbfe6_0001	R/W	I2S configuration register	0x0
IISState	0xbfe6_0002	R/W	I2S status register	0x0
IISRxData	0xbfe6_0003	R/W	I2S data reception register	0x0
IISTxData	0xbfe6_0004	R/W	I2S data transmission register	0x0
AC97				
CSR	0xbfe6_0000	R/W	Configuration status register	0x0
OCC0	0xbfe6_0004	R/W	Output channel configuration register 0	0x4141
OCC1	0xbfe6_0008		Reserved	
OCC2	0xbfe6_000c		Reserved	
ICC	0xbfe6_0010	R/W	Input channel configuration register	0x410000
CODEC_ID	0xbfe6_0014		Codec ID register	
CRAC	0xbfe6_0018		Codec register access command	0x0
OC0	0xbfe6_0020		Output sound track 0	
OC1	0xbfe6_0024		Output sound track 1	

OC2	0xbfe6_0028		Reserved	
OC3	0xbfe6_002c		Reserved	
OC4	0xbfe6_0030		Reserved	
OC5	0xbfe6_0034		Reserved	
OC6	0xbfe6_0038		Reserved	
OC7	0xbfe6_003c		Reserved	
OC10	0xbfe6_0040		Reserved	
IC0	0xbfe6_0044		Reserved	
IC1	0xbfe6_0048		Reserved	
IC2	0xbfe6_004c		Input sound track 2	
INTRAW	0xbfe6_0054	R/W	Interrupt status register	
INTM	0xbfe6_0058	R/W	Interrupt mask	0x0
INT_CLR	0xbfe6_005c	R	Interrupt status / clear register	0x0
INT_OC_CLR	0xbfe6_0060	R	OC Interrupt clear register	0x0
INT_IC_CLR	0xbfe6_0064	R	IC Interrupt clear register	0x0
INT_CW_CLR	0xbfe6_0610	R	CODEC write interrupt clear register	0x0
INT_CR_CLR	0xbfe6_006c	R	CODEC read interrupt clear register	0x0
RTC				
sys_toywrite0	0xbfe6_4024	W	TOY low 32-bit value read-in	
sys_toywrite1	0xbfe6_4028	W	TOY high 32-bit value read-in	
sys_toyread0	0xbfe6_402C	R	TOY low 32-bit value read-out	
sys_toyread1	0xbfe6_4030	R	TOY high 32-bit value read-out	
SDIO interface				
sdi_con	0xbfe6_c000	R/W	SDIO control register	0x0
sdi_pre	0xbfe6_c004	R/W	SDIO prescale register	0x1
sdi_cmd_arg	0xbfe6_c008	R/W	SDIO command parameter register	0x0
sdi_cmd_con	0xbfe6_c00c	R/W	SDIO command control register	0x0
sdi_cmd_sta	0xbfe6_c010	R	SDIO command status register	0x0
sdi_rsp0	0xbfe6_c014	R/W	SDIO response register 0	0x0
sdi_rsp1	0xbfe6_c018	R/W	SDIO response register 1	0x0
sdi_rsp2	0xbfe6_c01c	R/W	SDIO response register 2	0x0
sdi_rsp3	0xbfe6_c020	R/W	SDIO response register 3	0x0
sdi_dtimer	0xbfe6_c024	R/W	SDIO timing register	0x1388
sdi_bsize	0xbfe6_c028	R/W	SDIO block size register	0x0
sdi_dat_con	0xbfe6_c02c	R/W	SDIO data control register	0x0
sdi_dat_cnt	0xbfe6_c030	R/W	SDIO data counter	0x0

sdi_dat_sta	0xbfe6_c034	R	SDIO data status register	0x0
sdi_fsta	0xbfe6_c038	R	SDIO FIFO status register	0x0
sdi_int_mask	0xbfe6_c03c	R/W	SDIO interrupt mask register	0x0
sdi_wdat	0xbfe6_c040	R/W	SDIO (data register)	0x0
sdi_int_en	0xbfe6_c064	RW	SDIO interrupt enable register	0x0
ADC interface				
adc_cnt	0xbfe7_4000	R/W	Frequency division and sampling interval register	0x400010
adc_s_ctrl	0xbfe7_4004	R/W	Single sampling control register	0x0
adc_c_ctrl	0xbfe7_4008	R/W	Continuous sampling control register	0x0
x_range	0xbfe7_4010	R/W	Touch screen X direction threshold	0x3ff0000
y_range	0xbfe7_4014	R/W	Touch screen Y direction threshold	0x3ff0000
awatchdog_range	0xbfe7_4018	R/W	Analog watchdog threshold	0x3f0000f
axis	0xbfe7_401c	R/W	Touch screen coordinates	0x0
adc_s_dout0	0xbfe7_4020	R/W	Result of single sampling by channel 0 and channel 1	0x0
adc_s_dout1	0xbfe7_4024	R/W	Result of single sampling by channel 2 and channel 3	0x0
adc_c_dout	0xbfe7_4028	R/W	Continuous sampling results	0x0
adc_debounce_cnt	0xbfe7_402c	R/W	Touch screen debouncing time	0x640
adc_int	0xbfe7_4030	R/W	ADC interrupt flag and control	0x0
NAND				
NAND_CMD	0Xbfe7_8000	R/W	NAND command register	0x0
ADDR_C	0Xbfe7_8004	R/W	NAND page offset address register	0x0
ADDR_R	0Xbfe7_8008	R/W	NAND page address register	0x0
NAND_TIMING	0Xbfe7_800C	R/W	NAND timing sequence register	0x412
ID_L	0Xbfe7_8010	R	NAND low ID register	0x0
STATUS & ID_H	0Xbfe7_8014	R	NAND high ID register	0x0
NAND_PARAMETER	0Xbfe7_8018	R/W	NAND grain parameter register	0x
NAND_OP_NUM	0Xbfe7_801C	R/W	NAND reading and writing number register	0x800
CS_RDY_MAP	0Xbfe7_8020	R/W	NAND grain RDY	0x0

			Signal	
DMA access address	0Xbfe7_8040	R/W	NAND read-write data register	0x0
CAMERA interface				
DMA_ADDR0_CONFIG	0xbc28_0000	R/W	Frame buffer base address 0	0x0
DMA_ADDR1_CONFIG	0xbc28_0008	R/W	Frame buffer base address 1	0x0
DMA_ADDR2_CONFIG	0xbc28_0010	R/W	Frame buffer base address 2	0x0
DMA_ADDR3_CONFIG	0xbc28_0018	R/W	Frame buffer base address 3	0x0
Camif_config_pix	0xbc28_0020	R/W	Floating resolution ratio pixel	0x0
Camif_config_uoffset	0xbc28_0028	R/W	U base address	0x0
Camif_config_voffset	0xbc28_0030	R/W	V base address	0x0
Camif_config	0xbc28_0038	R/W	Status register	0x0
HCNTR interface				
hcntr_ctrl	0xbfe7_c000	R/W	Timer control register	0x0

4 Clock Architecture

4.1 Clock Architecture

The clock architecture of Loongson 1C is shown in the figure below, and the clock from XTALI/O is sent to two USBPHY and one PLL. After frequency division, PLL generates the work clock of main modules such as CPU, SDRAM, MAC and USB; modules such as USB, MAC and OTG use their respective clock in interface (or reference clock)

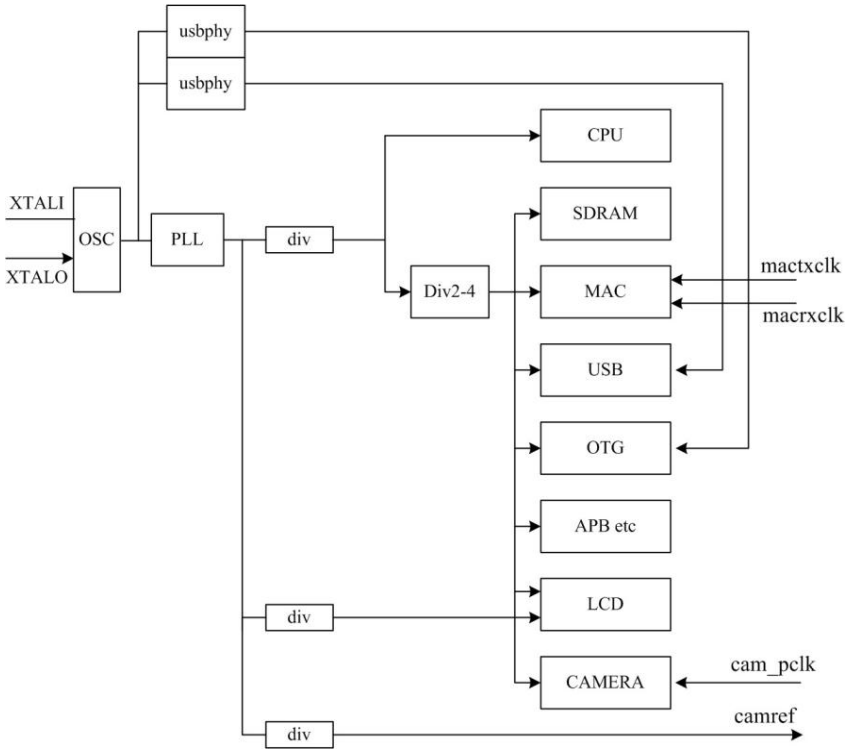

Figure 4-1 System clock architecture

4.2 Clock Signal Description

Table 4-1 has introduced all clock pins of Loongson 1C.

Table 4-1 Loongson 1C clock signal

Signal name	Frequency (Hz)	Type	Description
XTALI XTALO		I/O	PLL and USBPHY reference clocks are connected to 24MHz crystal.
MACTXCLK		I	MAC reference clock transmission
MACRXCLK		I	MAC reference clock reception
CAM_PCLK		I	Camera pixel clock

5 Chip Configuration and Control

5.1 Address space allocation

The address space of Loongson 1C is divided into three levels, including the address space of modules above the first-level AXI crossbar module, that of all modules under AXI_MUX, and that of on-APB modules.

Table 5-1 Space assignment of AXI modules

Address space	Equipment	Note
0x0000_0000 – 0x0fff_ffff	SDRAM	256MB
0xbc28_0000 – 0xbc2f_ffff	CAMERA_IF	512K
0xbc30_0000 – 0xbc3f_ffff	DC	1MB
0xbf00_0000 – 0xbfff_ffff	AXI MUX	16MB

Table 5-2 Address assignment of all AXI modules

Address space	Equipment	Note
0xbd00,0000 – 0xbd7f,ffff	SPI0-memory	8MB
0xbe00,0000 – 0xbe3f,ffff	SPI1-memory	4MB
0xbfc0_0000 – 0xbfcf_ffff	Boot	1MB is mapped to SPI or NAND by means of system booting.
0xbfd0_0000 – 0xbfdf_ffff	CONFREG	1MB
0xbfe0_0000 – 0xbfe0_ffff	OTG	64KB
0xbfe1_0000 – 0xbfe1_ffff	MAC	64KB
0xbfe2_0000 – 0xbfe2_ffff	USB	64KB
0xbfe4_0000 – 0xbfe7_ffff	APB-devices	256KB
0xbfe8,0000 – 0xbfeb,ffff	SPI0-IO	256KB
0xbfec,0000 – 0xbfef,ffff	SPI1-IO	256KB

Table 5-3 Address assignment of all AXI modules

Address space	Modules	Note
0xbfe4_0000-0xbfe4_3fff	UART0	16KB
0xbfe4_4000-0xbfe4_7fff	UART1	16KB
0xbfe4_8000-0xbfe4_bfff	UART2	16KB
0xbfe4_c000-0xbfe4_c0ff	UART3	16KB
0xbfe4_c400-0xbfe4_c4ff	UART4	256B
0xbfe4_c500-0xbfe4_c5ff	UART5	256B
0xbfe4_c600-0xbfe4_c6ff	UART6	256B
0xbfe4_c700-0xbfe4_c7ff	UART7	256B
0xbfe4_c800-0xbfe4_c8ff	UART8	256B
0xbfe4_c900-0xbfe4_c9ff	UART9	256B
0xbfe4_ca00-0xbfe4_caff	UART10	256B
0xbfe4_cb00-0xbfe4_cbff	UART11	256B
0xbfe5_0000-0xbfe5_3fff	CAN0	16KB
0xbfe5_4000-0xbfe5_7fff	CAN1	16KB
0xbfe5_8000-0xbfe5_bfff	I2C-0	16KB
0xbfe5_c000-0xbfe5_ffff	PWM	16KB
0xbfe6_0000-0xbfe6_3fff	AC97/I2S	16KB
0xbfe6_4000-0xbfe6_7fff	RTC	16KB
0xbfe6_8000-0xbfe6_bfff	I2C-1	16KB
0xbfe6_c000-0xbfe6_ffff	SDIO	16KB
0xbfe7_0000-0xbfe7_3fff	I2C-2	16KB
0xbfe7_4000-0xbfe7_7fff	ADC	16KB
0xbfe7_8000-0xbfe7_bfff	NAND	16KB

0xbfe7_c000-0xbfe7_ffff	HCNTR	16KB

5.2 Chip Configuration Register (CONFREG)

There is a dedicated configuration register module (CONFREG) in Loongson 1C chip, which is used for some basic configurations and multiplex relations in chip. The following is a list of registers and instructions.

5.2.1 PLL/SDRAM Frequency configuration register

Register name	Address	R/W	Function description	Reset value
START_FREQ	0xbfe78030	R/W	PLL Configuration frequency and SDRAM frequency coefficient	

START_FREQ	Bit	Default values	Description
PLL_VALID	31	0	PLL valid bit of clock multiplier factor
Reserved	30:24	0	
FRAC_N	23:16	0	PLL fractional part of clock multiplier factor
M_PLL	15:8	Configured by NAND_D [3:0]	Integer part of PLL clock multiplier factor (theoretically, it may reach 255, but had better not exceed 100)
Reserved	7:4	0	
RST_TIME	3:2		Resetting time after PLL frequency configuration completion 00: Indicate no reset 01: Indicate 0x100 CLK 10: Indicate 0x400 CLK 10: Indicate 0xff0 CLK
SDRAM_DIV	1:0		Frequency division factor from CPU to SDRAM 00: Indicate 2 fractional frequency 01: Indicate 4 fractional frequency 10 or 11: Indicate 3 fractional frequency

Notes: the frequency division factor N of PLL is fixed as 4, and the calculation formula of PLL frequency is shown as follows:

Freq_PLL = XIN *(M_PLL + FRAC_N)/4

5.2.2 CPU/CAMERA/DC frequency configuration register

Register name	Address	Read / Write (R / W)	Function description	Reset value
CLK_DIV_PARAM	0xbfe7.8034	R/W	CPU/CAMERA/DC frequency division factor	

CLK_DIV_PARAM	Bit	Default values	Description
PIX_DIV	31:24	0x24	DC frequency coefficient of pixel clock PIX_DIV[7] is the significant bit value of configuration parameter. When it's 1, PIX_DIV[6:0] is valid.

			PIX_DIV[6:0] is the frequency division factor. When it's 0, there is no frequency division, and it ranges from 1 to 27.
CAM_DIV	23:16	0x24	CAMERA clock frequency coefficient CAM_DIV[7] is the significant bit of configuration parameter. When it's 1, CAM_DIV[6:0] is valid. CAM_DIV[6:0] is the frequency division factor. When it's 0, there is no frequency division, and it ranges from 1 to 127.
CPU_DIV	15:8	0x2	CPU clock frequency coefficient CPU_DIV[7] is the significant bit of configuration parameter. When it's 1, CPU_DIV[6:0] is valid. CPU_DIV[6:0] is the frequency division factor. When it's 0, there is no frequency division, and it ranges from 1 to 127.
Reserved	7:6	0	
PIX_DIV_VALID	5	0	DC pixel clock frequency coefficient valid
PIX_SEL	4	0	DC pixel clock selection signal When it's 1, select fractional frequency clock When it's 0, select the crystal oscillator, and input clock (bypass mode)
CAM_DIV_VALID	3	0	CAMERA valid clock frequency coefficient
CAM_SEL	2	0	CAMERA clock selection signal When it's 1, select fractional frequency clock When it's 0, select the crystal oscillator, and input clock (bypass mode)
CAM_DIV_VALID	1	0	CPU valid clock frequency coefficient
CAM_SEL	0	0	CPU clock selection signal When it's 1, select fractional frequency clock When it's 0, select the crystal oscillator, and input clock (bypass mode)

Freq_PIX = Freq_PLL/PIX_DIV;
Freq_CAM = Freq_PLL/CAM_DIV;
Freq_CPU = Freq_PLL/CPU_DIV;
Freq_SDRAM = Freq_CPU/SDRAM_DIV;

5.2.3 SDRAM parameter register

Register name	Address	Read / Write (R / W)	Function description	Reset value
SD_CONFIG[31:0]	0xbfd0_0410	R/W	SDRAM parameter configuration register	0x001438a3
SD_CONFIG[63:32]	0xbfd0_0414	R/W	SDRAM parameter configuration	0x80000080

			register	

See Chapter 7 for instructions and configuration of SDRAM parameter register

5.2.4 SHUT_CTRL register

Register name	Address	Read / Write (R / W)	Function description	Reset value
shut_ctrl	0xbfd0_0420	R/W	Each module switch register	0x0

SHUT_CTRL	Bit	Default values	Description
UART_split	31:30	0	Full-function serial port uart0 partition scheme. 00: Used as full-function serial port 01: Used as 2 four-wire serial ports
OUTPUT_CLK	29:26	0	Clock output configuration. Each bit indicates a clock output When the 0bit is 1, it indicates the PIX_CLK output of DC; when the 1st bit is 1, it indicates the CAMERA clock output from SPI0_CS pin; when the 2nd bit is 1, it indicates the CAMERA clock output from PWM0 pin; when the 3rd bit is 1, it indicates the clock output of crystal clock.
ADC_shut	25	0	ADC module shutdown, valid at 1
SDIO_shut	24	0	SDIO module shutdown, valid at 1
DMA2_shut	23	0	DMA2 module shutdown, valid at 1
DMA1_shut	22	0	DMA1 module shutdown, valid at 1
DMA0_shut	21	0	DMAO module shutdown, valid at 1
SPI1_shut	20	0	SPI1 module shutdown, valid at 1
SPI0_shut	19	0	SPI0 module shutdown, valid at 1
I2C2_shut	18	0	I2C2 module shutdown, valid at 1 In addition, for the UART0 full-function multiplex configuration bit, please refer to 5.2.6 UART multiplex configuration register
I2C1_shut	17	0	I2C1 module shutdown, valid at 1
I2C0_shut	16	0	I2C0 module shutdown, valid at 1
AC97_shut	15	0	AC97 module shutdown, valid at 1
I2S_shut	14	0	I2C module shutdown, valid at 1
UART3_shut	13	0	UART3 module shutdown, valid at 1
UART2_shut	12	0	UART2 module shutdown, valid at 1
UART1_shut	11	0	UART1 module shutdown, valid at 1
UART0_shut	10	0	UART0 module shutdown, valid at 1
CAN1_shut	9	0	CAN1 module shutdown, valid at 1
CAN0_shut	8	0	CAN0 module shutdown, valid at 1
ECC_shut	7	0	NAND ECC function off, and when it's 1, it's effective.
MAC_shut	6	0	MAC module shutdown, valid at 1
USBHOST_shut	5	0	USBHOST module shutdown, valid at 1
USBOTG_shut	4	0	USBOTG module shutdown, valid at 1

SDRAM_shut	3	0	SDRAM module shutdown, valid at 1
SRAM_shut	2	0	SRAM module shutdown, valid at 1
CAM_shut	1	0	CAMERA module shutdown, valid at 1
LCD_shut	0	0	LCD module shutdown, valid at 1

5.2.5 MISC_CTRL register

Register name	Address	Read / Write (R / W)	Function description	Reset value
misc_ctrl	0xbfe6_4024	R/W	Multiplexing function register	

MISC_CTRL	Bit	Default values	Description
USBHOST_RSTn	31	0	USBHOST module software reset
PHY_INTF_SEL_i	30:28	0	MAC module MII interface configuration signal 000: MII mode 100: RMII mode
Reserved	27:26	0	
AC97_EN	25	0	AC97 and I2S multiplex options. When the bit is 1, AC97 is used. When the bit is 0, I2S is used.
SDIO_DMA_EN	24:23	0	SDIO uses DMA. When the bit is 0, DMA isn't used. When the bit is 1, DMA0 is used. When the bit is 2, DMA1 is used. When the bit is 3, DMA2 is used.
ADC_DMA_EN	22	0	ADC uses DMA, When the bit is 1, it's significant.
Reserved	21:18	0	
SDIO_USE_SPI1	17	0	SDIO uses SPI1 pin. When the bit is 1, it's signifant.
SDIO_USE_SPI0	16	0	SDIO uses SPI0 pin. When the bit is 1, it's significant.
SRAM_CTRL	15:0	0	SRAM configuration parameters. See SRAM.

5.2.6 Cpu_throt register

Register name	Address	Read / Write (R / W)	Function description	Reset value
cpu_throt	0xbfe7_c010	R/W	CPU dynamic downclock control register	0x0

cpu_throt	Bit	Default values	Description
Reserved	31:4	0	
cpu_throt	3:0	0xf	CPU frequency reduction coefficients. This configuration is only effective for CPU frequency, and has no influence on bus clock and SDRAM clock. cpu_throt is described as follows:

			0xf: Keep CPU frequency unchanged. 0xe: Reduce to 15/16 of the original frequency 0xd: Reduce to 14/16 of the original frequency 0xc: Reduce to 13/16 of the original frequency 0xb: Reduce to 12/16 of the original frequency 0xa: Reduce to 11/16 of the original frequency 0x9: Reduce to 10/16 of the original frequency 0x8: Reduce to 9/16 of the original frequency 0x7: Reduce to 8/16 of the original frequency 0x6: Reduce to 7/16 of the original frequency 0x5: Reduce to 6/16 of the original frequency 0x4: Reduce to 5/16 of the original frequency 0x3: Reduce to 4/16 of the original frequency 0x3: Reduce to 3/16 of the original frequency 0x1: Reduce to 2/16 of the original frequency 0x0: Reduce to 1/16 of the original frequency

5.2.7 UART multiplex configuration register

Register name	Address	Read / Write (R / W)	Function description	Reset value
uart0_full_func	0xbfd0_0420	R/W	Whether to multiplex uart4~uart6 into the full function or self function of uart0	0x0
uart8_full_func	0xbfe4_c904	R/W	Whether to multiplex uart9~uart11 into the full function or self function of uart8	0x0

UART0_FULL_FUNC	Bit	Default values	Description
	31:19	0	misc_ctrl[31:19]
uart0_full_func	18	0	When the bit is 0, uart4~uart6 is used as the self signal of uart4~6, and I2C2 module is opened. When the bit is 1, uart4~uart6 is used as the self signal of uart0, and I2C2 module

			is opened.
	17:0	0	misc_ctrl[17:0]

UART8_FULL_FUNC	Bit	Default values	Description
	7:1	0	In common with MSR [7:1]
uart8_full_func	0	0	When the bit is 0, uart9~uart11 is used as the self signal of uart8~11 When the bit is 1, uart9~uart11 is used as the self signal of uart8, and I2C2 module is closed.

5.2.8 GPIO0 Configuration Register (corresponding GPIO[31:0])

Register name	Address	Read / Write (R / W)	Function description	Reset value
GPIO_CFG0	0xbfd0_10c0	R/W	GPIO0 configuration register 1 indicates the configuration is GPIO, and 0 indicates ineffective.	0xfc00_3f3f
GPIO_EN0	0xbfd0_10d0	R/W	GPIO0 output enable register 1 indicates the input, and 0 indicates the configuration is input.	0xfc00_3f3f
GPIO_IN0	0xbfd0_10e0	R	GPIO0 input register	0x0
GPIO_OUT0	0xbfd0_10f0	R/W	GPIO0 output register High output at 1 Low output at 0	0x0

If the GPIO[16] output is configured 1, it's necessary to configure GPIO_CFG[16] as 1, then GPIO_EN[16] as 1, and GPIO_OUT[16] as 1. Similarly, GPIO0~GPIO127 input or output can be configured.

5.2.9 GPIO1 configuration register (corresponding GPIO[63:32])

Register name	Address	Read / Write (R / W)	Function description	Reset value
GPIO_CFG1	0xbfd0_10c4	R/W	GPIO1 configuration register 1 indicates the configuration is GPIO, and 0 indicates ineffective.	0x0
GPIO_EN1	0xbfd0_10d4	R/W	GPIO1 output enable register 1 indicates the input, and 0 indicates the configuration is input.	0x0
GPIO_IN1	0xbfd0_10e4	R	GPIO1 input register	0x0
GPIO_OUT1	0xbfd0_10f4	R/W	GPIO1 output register High output at 1 Low output at 0	0x0

5.2.10 GPIO2 configuration register (corresponding GPIO[95:64])

Register name	Address	Read / Write (R / W)	Function description	Reset value
GPIO_CFG2	0xbfd0_10c8	R/W	GPIO2 configuration register 1 indicates the configuration is GPIO, and 0 indicates ineffective.	0x0
GPIO_EN2	0xbfd0_10d8	R/W	GPIO2 output enable register 1 indicates the input, and 0 indicates the configuration is input.	0x0
GPIO_IN2	0xbfd0_10e8	R	GPIO2 input register	0x0
GPIO_OUT2	0xbfd0_10f8	R/W	GPIO2 output register High output at 1 and low output at 0	0x0

5.2.11 GPIO3 configuration register (corresponding GPIO[127:96])

Register name	Address	Read / Write (R / W)	Function description	Reset value
GPIO_CFG3	0xbfd0_10cc	R/W	GPIO3 configuration	0x0
			Register 1 indicates the configuration is GPIO, and 0 indicates ineffective.	
GPIO_EN3	0xbfd0_10dc	R/W	GPIO3 output enable register 1 indicates the input, and 0 indicates the configuration is input.	0x0
GPIO_IN3	0xbfd0_10ec	R	GPIO3 input register	0x0
GPIO_OUT3	0xbfd0_10fc	R/W	GPIO3 output register High output at 1 Low output at 0	0x0

5.2.12 PAD[31:0] pin multiplex relation configuration register

Register name	Address	Read / Write (R / W)	Function description	Reset value
CBUS_FIRST0	0xbfd0_11c0	R/W	PAD[31:0] 1st multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 1st multiplex, and when the bit is 1, it indicates ineffective.	0x0
CBUS_SECOND0	0xbfd0_11d0	R/W	PAD[31:0] 2nd multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 2nd multiplex, and when the bit is 0, it indicates ineffective.	0x0
CBUS_THIRD0	0xbfd0_11e0	R/W	PAD [31:0] No.	0x0

			The 3rd multiplex register, when the bit is 1, it indicates the corresponding PAD is configured as the 3rd multiplex, and when the bit is 0, it indicates ineffective.	
CBUS_FOURTHT0	0xbfd0_11f0	R/W	PAD[31:0] 4th multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 4th multiplex, and when the bit is 0, it indicates ineffective.	0x0
CBUS_FIFTHT0	0xbfd0_1200	R/W	PAD[31:0] 5th multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 5th multiplex, and when the bit is 0, it indicates ineffective.	0x0

1C chip pin has several multiplex relations, and has six functions and one GPIO multiplex relation at most. See multiplex relation table in Chapter VII of data book. The multiplexed relationship of each pin is prioritized as follows:
1st multiplex>2nd multiplex>3rd multiplex>4th multiplex>5th multiplex>GPIO multiplex>default function
For example, to use the 4th multiplex function of PAD[21], it's necessary to configure CBUS_FIRST0[21]~ CBUS_THIRD0[21] as 0 and CBUS_FOURTH0[21] as 1. If to use default function, it's necessary to configure CBUS_FIRST0[21]~ CBUS_FOURTH0[21] and GPIO[21] as 0.

5.2.13 PAD[63:32] pin multiplex relation configuration register

Register name	Address	Read / Write (R / W)	Function description	Reset value
CBUS_FIRST1	0xbfd0_11c4	R/W	PAD[63:32] the 1st multiplex register, bit	0x0
			When the bit is 1, it indicates that corresponding PAD configuration is the 1st multiplex. When the bit is 0, it indicates ineffective.	
CBUS_SECOND1	0xbfd0_11d4	R/W	PAD[63:32] 2nd multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 2nd multiplex, and when the bit is 0, it indicates ineffective.	0x0
CBUS_THIRD1	0xbfd0_11e4	R/W	PAD[63:32] 3rd multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 3rd multiplex, and when the bit is0, it indicates ineffective.	0x0
CBUS_FOURTHT1	0xbfd0_11f4	R/W	PAD[63:32] 4th multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 4th multiplex, and when the bit is 0, it indicates ineffective.	0x0
CBUS_FIFTHT1	0xbfd0_1204	R/W	PAD[63:32] 5th multiplex	0x0

			register. When the bit is 1, it indicates the corresponding PAD is configured as the 5th multiplex, and when the bit is 0, it indicates ineffective.	

5.2.14 PAD[95:64] pin multiplex relation configuration register

Register name	Address	Read / Write (R / W)	Function description	Reset value
CBUS_FIRST2	0xbfd0_11c8	R/W	PAD[95:64] 1st multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 1st multiplex, and when the bit is 1, it indicates ineffective.	0x0
CBUS_SECOND2	0xbfd0_11d8	R/W	PAD[95:64] 2nd multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 2nd multiplex, and when the bit is 0, it indicates ineffective.	0x0
CBUS_THIRD2	0xbfd0_11e8	R/W	PAD[95:64] 3rd multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 3rd multiplex, and when the bit is0, it indicates ineffective.	0x0
CBUS_FOURTHT2	0xbfd0_11f8	R/W	PAD[95:64] 4th multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 4th multiplex, and when the bit is 0, it indicates ineffective.	0x0
CBUS_FIFTHT2	0xbfd0_1208	R/W	PAD [95:64] No.	0x0
			The 5th multiplex register, when the bit is 1, it indicates the corresponding PAD is configured as the 5th multiplex, and when the bit is 0, it indicates ineffective.	

5.2.15 PAD[127:96] pin multiplex relation configuration register

Register name	Address	Read / Write (R / W)	Function description	Reset value
CBUS_FIRST3	0xbfd0_11cc	R/W	PAD[127:96] 1st multiplex register	0x0
CBUS_SECOND3	0xbfd0_11dc	R/W	PAD[127:96] 2nd multiplex register	0x0
CBUS_THIRD3	0xbfd0_11ec	R/W	PAD[127:96] 3rd multiplex register	0x0
CBUS_FOURTHT3	0xbfd0_11fc	R/W	PAD[127:96] 4th multiplex register	0x0
CBUS_FIFTHT3	0xbfd0_120c	R/W	PAD[127:96] 5th multiplex register. When the bit is 1, it indicates the corresponding PAD is configured as the 5th multiplex, and when the bit is 0, it indicates ineffective.	0x0

5.3 Interrupt Configuration Register

There are five groups in total in interrupt register which correspond to five interrupt bits in CAUSE register of CPU. Each group consists of status register, enable register, set register, clear register, level selection register and edge selection register. Each bit of these five registers is in one-to-one correspondence. All PIO[104:0] can be used as interrupt status register, and special interrupt register is distributed in INT0_SR and INT1_SR.
The first group of interrupt registers

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT0_SR	0xbfd0_1040	R	When the bit of interrupt status register 0 is 1, it indicates that the corresponding bit generates interrupt. When it's 0, it indicates no interrupt.	0x0
INT0_EN	0xbfd0_1044	R/W	When the bit of interrupt status register 0 is 1, it indicates that the corresponding bit of enable generates interrupt. When it's 0, it indicates it's forbidden.	0x0
INT0_SET	0xbfd0_1048	R/W	When the bit of interrupt status register 0 is 1, it indicates the interrupt setting. When it's o, it's ineffective.	0x0
INT0_CLR	0xbfd0_104C	R/W	When the bit of interrupt clear register is 1, it indicates clearing interrupt. When it's o, it's ineffective.	0x0
INT0_POL	0xbfd0_1050	R/W	Interrupt polarity selection register 0 When int0_edge is configured as the level trigger, the bit 1 indicates the high level triggered interrupt. When it's 0, it indicates the low level trigger. When int0_edge is configured as edge trigger. When it's 1, it indicates the up edge trigger interrupt. When it's 0, it indicates the down edge trigger.	0x0
INT0_EDGE	0xbfd0_1054	R/W	Interrupt edge selection register 0 When the bit is 1, it indicates the edge trigger, and when it's 0, it indicates the level trigger.	0x0

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT0_SR	0xbfd0_1040	R	Interrupt status register 0	0x0

INT0_SR	Bit	Default values	Description
NAND_int	31	0	NAND interrupt status bit
SDIO_int	30	0	SDIO interrupt status bit
UART3_int	29	0	UART3 interrupt status bit

Reserved	28:24	0	
RTC_int	23:21	0	RTC interrupt status bit
PWM_int	20:17	0	Corresponding 4-channel PWM interrupt status bit
Reversed	16	0	
DMA_int	15:13	0	Corresponding 3-channel DMA interrupt status bit
Reversed	12:11	0	
I2S_AC97_int	10	0	I2S or AC97 interrupt status bit. When ac97_en is 1, the bit is AC97 interrupt status bit, or it is I2S interrupt status bit.
SPI1_int	9	0	SPI1 interrupt status bit
SPI0_int	8	0	SPI0 interrupt status bit
CAN1_int	7	0	CAN1 interrupt status bit
CAN0_int	6	0	CAN0 interrupt status bit
UART2_int	5	0	UART2 interrupt status bit
UART1_int	4	0	UART1 interrupt status bit
UART0_int	3:0	0	UART0 interrupt status bit

The second group of interrupt registers

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT1_SR	0xbfd0_1058	R	Interrupt status register 1 In common with INT0_SR	0x0
INT1_EN	0xbfd0_105c	R/W	Interrupt enable register 1 In common with INT0_EN	0x0
INT1_SET	0xbfd0_1060	R/W	Interrupt setting register 1 In common with INT0_SET	0x0
INT1_CLR	0xbfd0_1064	R/W	Interrupt clear register 1 In common with INT0_CLR	0x0
INT1_POL	0xbfd0_1068	R/W	Interrupt polarity selection register 1 In common with interrupt polarity selection register 0	0x0
INT1_EDGE	0xbfd0_106c	R/W	Interrupt edge selection register 1 Interrupt edge selection register 0	0x0

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT1_SR	0xbfd0_1058	R	Interrupt status register 1	

INT1_SR	Bit	Default values	Description
Gpio[105:96]	31:22	0	GPIO[105:96] as interrupt input, interrupt status bit
Reserved	21:20	0	
I2C_int0	19	0	I2C0 interrupt status bit
I2C_int1	18	0	I2C1 interrupt status bit
I2C_int2	17	0	I2C2 interrupt status bit
Reserved	16	0	
UART11_int	15	0	UART11 interrupt status bit
UART10_int	14	0	UART10 interrupt status bit
UART9_int	13	0	UART9 interrupt status bit
UART8_int	12:9	0	UART8 interrupt status bit

UART7_int	8	0	UART7 interrupt status bit
UART6_int	7	0	UART6 interrupt status bit
UART5_int	6	0	UART5 interrupt status bit
UART4_int	5	0	UART4 interrupt status bit

cam_int	4	0	CAMERA interrupt status bit
mac_int	3	0	MAC interrupt status bit
otg_int	2	0	OTG interrupt status bit
ohci_int	1	0	USB_OHCI interrupt status bit
ehci_int	0	0	USB_EHCI interrupt status bit

The third group of interrupt registers

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT2_SR	0xbfd0_1070	R	Interrupt status register 2 In common with INT0_SR	0x0
INT2_EN	0xbfd0_1074	R/W	Interrupt enable register 2 In common with INT0_EN	0x0
INT2_SET	0xbfd0_1078	R/W	Interrupt setting register 2 In common with INT0_SET	0x0
INT2_CLR	0xbfd0_107c	R/W	Interrupt clear register 2 In common with INT0_CLR	0x0
INT2_POL	0xbfd0_1080	R/W	Interrupt polarity selection register 2 Interrupt polarity selection register 0	0x0
INT2_EDGE	0xbfd0_1084	R/W	Interrupt edge selection register 2 In common with interrupt edge selection register 2	0x0

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT2_SR	0xbfd0_1070	R	Interrupt status register 2	0x0

INT2_SR	Bit	Default values	Description
GPIO[31:0]	31:0	0	GPIO[31:0] as interrupt input, interrupt status bit

The fourth group of interrupt registers

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT3_SR	0xbfd0_1088	R	Interrupt status register 3 In common with INT0_SR	0x0
INT3_EN	0xbfd0_108c	R/W	Interrupt enable register 3 In common with INT0_EN	0x0
INT3_SET	0xbfd0_1090	R/W	Interrupt setting register 3 In common with INT0_SET	0x0
INT3_CLR	0xbfd0_1094	R/W	Interrupt clear register 3 In common with INT0_CLR	0x0
INT3_POL	0xbfd0_1098	R/W	Interrupt polarity selection register 3 In common with INT0_POL	0x0
INT3_EDGE	0xbfd0_109c	R/W	Interrupt edge selection register 3 In common with INT0_EDGE	0x0

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT3_SR	0xbfd0_1088	R	Interrupt status register 3	0x0

INT3_SR	Bit	Default values	Description
GPIO[64:32]	31:0	0	GPIO[63:32] is as interrupt input, interrupt status Bit

The fifth group of interrupt registers

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT4_SR	0xbfd0_10a0	R	Interrupt status register 4 In common with INT0_SR	0x0
INT4_EN	0xbfd0_10a4	R/W	Interrupt enable register 4 In common with INT0_EN	0x0
INT4_SET	0xbfd0_10a8	R/W	Interrupt setting register 4 In common with INT0_SET	0x0
INT4_CLR	0xbfd0_10ac	R/W	Interrupt clear register 4	0x0
			In common with	

			INT0_CLR	
INT4_POL	0xbfd0_10b0	R/W	Interrupt polarity selection register 4 In common with INT0_POL	0x0
INT4_EDGE	0xbfd0_10b4	R/W	Interrupt edge selection register 4 In common with INT0_EDGE	0x0

Register name	Address	Read / Write (R / W)	Function description	Reset value
INT4_SR	0xbfd0_10a0	R	Interrupt status register 4	0x0

INT4_SR	Bit	Default values	Description
GPIO[95:64]	31:0	0	GPIO[95:64] is as interrupt input, interrupt status Bit

6 SDRAM Controller

6.1 Overview

The SDRAM memory controller integrated by Loongson 1C processor implement general memory read/write/sleep operations, support 8/16bit data width, and the maximum capacity is 1GB (1C2 supports 2GB).

6.2 Register Description

SDRAM has one 64bit configuration register SD_CONFIG[63:0], and the effective one is [41:0]. The configuration register of system allocation is SD_CONFIG [63:0] and the address is 0x0410~0x0414. It's defined as follows:

Register name	Address	Read / Write (R / W)	Function description	Reset value
SD_CONFIG[31:0]	0xbfd0_0410	R/W	SDRAM parameter configuration register	0x00143803
SD_CONFIG[63:32]	0xbfd0_0414	R/W	SDRAM parameter configuration register	0x80000080

SD_CONFIG	Bit	Default values	Description
CONFIG_VALID	41		Valid configuration register
HANG_UP	40		Flag suspended bit
DEF_SEL	39		Adopt default configuration
TWR	38:37		Precharge time of grains after writing
TREF	36:25		Auto refresh period of grains
TRAS	24:21		Minimum line opening time of grains
TRFC	20:17		Auto refresh time of grains
TRP	16:14		Precharge time of grains
TCL	13:11		Data reading delay of grains
TRCD	10:8		Delayed line command to list command of grains
SD_BIT	7:6		Bit width of grains
SD_CSIZE	5:3	3'h0	Column numbers of grains
SD_RSIZE	2:0	3'h0	Line numbers of grains

6.3 Software Configuration Description

SD_CONFIG register is defined as follows:
1. SD_RSIZE, SD_CSIZE
The effective value of SD_RSIZE is 00, 01, 10 and 11 which correspond to 2K, 4K, 8K and 16K respectively.
The effective value of SD_CSIZE is 00, 01, 10, 11 and 111 which correspond to 512, 1K, 2K, 4K and 256 respectively.
Above two configurations need to correspond to particles, and the column number is larger than line number. Thus the effective configuration is:

Column/line	00	01	10	11
00	2Kx512	4Kx512	8Kx512 (not common)	16Kx512 (not common)
01	2Kx1K	4Kx1K	8Kx1K	16Kx1K (not common)

10	No	4Kx2K	8Kx2K	16Kx2K
11	No	No	8Kx4K	16Kx4K
111	2Kx256	4Kx256	8Kx256 (not common)	16Kx256 (not common)

2. SD_BIT
The effective value of SD_BIT is 00, 01 and 10 which correspond to 8bit, 16bit and 32bit respectively.

3. TRCD, TCL, TRP, TRFC, TRAS, TREF, TWR
These particles are related to the physical characteristics of particles, and are physical time which needs converting into cycle number based on frequency. Some parameters of typical frequency value are listed as follows:

Parameters /Frequency (MHZ)	150	133	100	75	33
TRCD	3	3	2	2	1
TCL	3	3	3	2	2
TRP	3	3	2	2	1
TRFC	9	8	6	5	2
TRAS	7	6	5	4	2
TREF	'h926	'h818	'h620	'h494	'h204
TWR	2	2	2	1	1

4. DEF_SEL
When the bit is 1, it adopts the default configuration (133MHZ configuration). When the bit is 0, it adopts the external input configuration. When the default configuration is adopted, the register configuration of external input is ineffective.

5. HANG_UP
When the bit is 1, it notifies that the controller enters in the suspende state, and after completing the operation in array, SDRAM enters into the sleep state, and exit from the sleep state after HANG_UP is 0. When it exits from the sleep state, it needs to refresh all lines by at least 240~480us. SD_CONFIG register only has one bit under normal work.

6. CONFIG_VALID

When the bit is 1, the register configuration is effective; when the bit is 1, it’s recommended to configure parameters first, and then set 1 bit high.

Notes: In the configuration of two registers, the low bit 0x410 must be written first, and then high 0x414. Or, when the SDRAM controller is writing 0x414, 0x410 initialization data will be seen as configuration parameter, and 0x410 data written later will be ineffective. In this way, SDRAM configuration is wrong and can’t work normally. It’s recommended to write the register three times, and the highest bit is set to 1 last time, and register enable is configured. (Valid bit in 0x414)

7 SRAM Controller

7.1 Overview

SRAM memory controller integrated by Loongson 1C processor is multiplexed with SDRAM pin, which support 32MB at most, and 8/16bits data width. SRAM controller can be used in IO device in the same interface sequence with SRAM.

7.2 Configuration Register

There is only one internal configuration register, and its configuration is shown as follows:

Register name	Address	Read / Write (R / W)	Function description	Reset value
MISC_CTRl[15:0]	0xbfe6_4024	R/W	SRAM parameter configuration register	0x0004

SRAM_CTRL	Bit	Default values	Description
SRAM_EN	15	0x0	SRAM enable. When the bit is 1, SDRAM interface is used as SRAM. When the bit is 0, it's used as SDRAM interface.
reserved	14:8	0x0	It must be 0 if reserved
SRAM_WIDTH16	7	0x0	ROM operation data with. When the bit is 1, it indicates 16 bits. When the bit is 0, it indicates 8 bits.
ROM_INIT_CNT	6:2	0x21	The count initial of RAM operation is used to adjust the phase of output signal, and ranges from 0 to 0x1f.
CLOCK_PERIOD	1:0	0x0	The count step value of SRAM operation is used to adjust the time length of adjusting output signal and operation speed. 00: Stepping at 1, the slowest 01: Stepping at 2 10: Stepping at 4 11: Stepping at 8, the fastest

8 Camera Interface

8.1 Overview

Camera Interface supports the input of ITU-R BT.601/656 YCbCr 8-bit standard and RGB565/888 8-bit standard. The input video frequency is 640x480 and 320x240 and any other pixel modes. It supports the zomming out by one time in 640x480 resolutions in RGB565\888 and ITU-R BT.601 modes. The rest pixel doesn't support the zooming out, and there is the output in the format of yuv4:2:2/rgb565/rgb888/rgb0888 by choice.

Functional characteristics of Camera interface controller includes:

- It supports the external interface of ITU-R BT.601/656 8-bit and RGB565/RGB888 8-bit modes.
- Support configuration by any resolution input;
- Only 640x480 supports the zooming out by one time.
- Output format: YCbCr 4:2:2, RGB565, RGB888 and RGB0888 (32bits). When the output format is RGB565/ YCbCr 4:2:2, the input pixels must be integral times of 32; the output format is RGB888/RGB0888, and the input pixel is integral times of 16.
- It supports the input of ITU-R BT.601/656 8-bit in any pixel into the output in the format of RGB (565/0888), and doesn't support the conversion of RGB input into YCbCr4:2:2 output;
- The output area has four sections, each of which can accommodate the address space of one frame image, and can configure the base address of address space, offset address of u and v component storage in the format of YCbCr4:2:2
- It support the conversion of RGB565 into RGB565;
- It support the conversion of RGB888 into RGB888 and RGB0888;
- It support the conversion of BT601 into RGB565, RGB0888 and YUV;
- It supports the conversion of BT656 into RGB565, RGB0888 and YUV;
- It supports the zooming out by one time of 640*480 pixel (except the format of TU-R BT.656);
- It supports the matrix display of the output in the format of RGB.

Interface block diagram of the module:

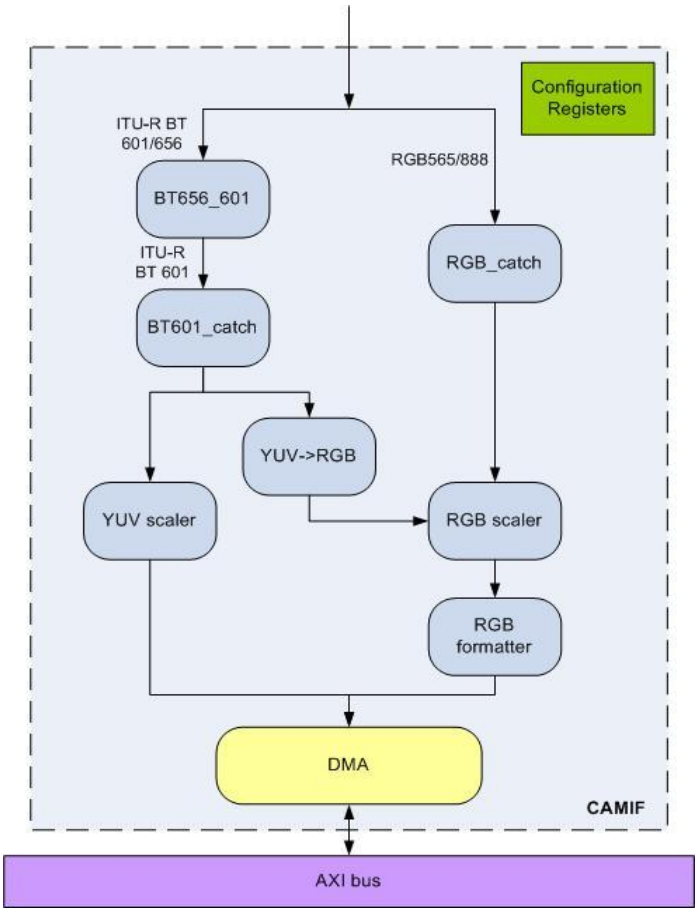

Figure 8-1 Camera interface (CAMIF) functional diagram

8.2 Interface Protocol

PCLK: 1bit input signal; Camera processor driven pixel clock.
VSYNC: 1bit input signal; Camera processor driven frame sync signal.
HREP: 1bit input signal; Camera processor driven frame sync signal.
DATA: 8bit input signal; pixel data initiated by Camera processor.
ITU-R BT.601 8-bit input sequence is shown in Figure 1. Therein, the data input sequence may be YCbY Cr or YCrYCb or CrYCbY or CbYCrY.
RGB565/RGB888 8-bit input sequence and ITU-R BT.601 8-bit input sequence are consistent, and the data input sequence is different. For RGB888, the data input sequence may be R G B or B G R. For RGB565, the data input sequence may be R5G3 G3B5 or B5G3 G3R5. RGB565/RGB888 and ITU-R BT.601 input mode can set the line effective and frame effective high and low levels based on low two bits of status register.

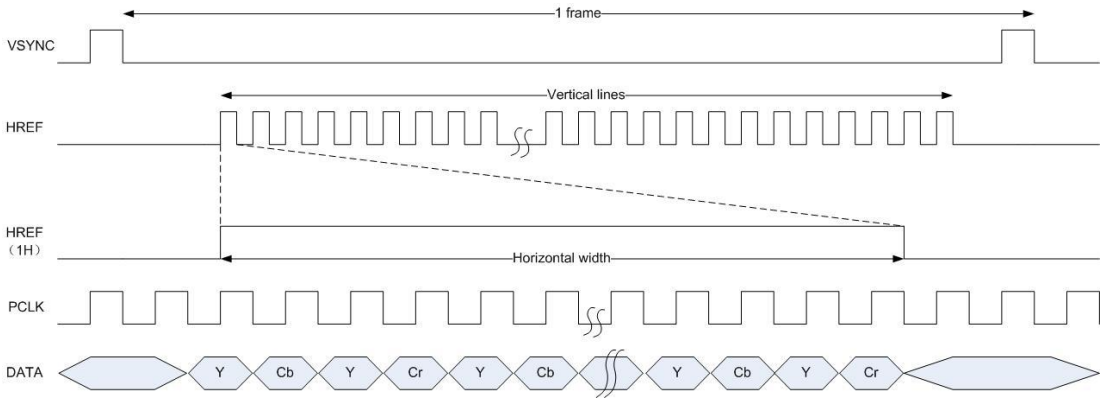

Figure 8-2 ITU-R BT.601 input sequence

ITU-R BT.656 input sequence is shown in Figure 8-3. Therein, the data input sequence can be Y CbYCr or YCrYCb or CrYCbY or CbYCrY. SAV is the line start code, and EAV is end code. The definition of reference code is shown in Table 8-1, and the definition of XY value is shown in Table 8-2. Only when XY is 80, 9D combination or C7, DA combination, it's effective line data.

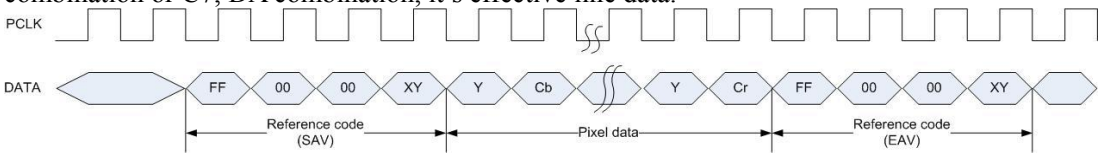

Figure 8-3 ITU-R BT.656 input sequence

Table 8-1 ITU-R BT.656 reference code

Data bit number	The first character (3FF)	The second character (000)	The third character (000)	The fourth character (XYZ)
7(MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0	1	0	0	P0

In Field 1, F is 0; in Field 2, it's 1.
V other positions 0; vertical blanking interval is 1
H is 0 in SAV and 1 in EAV.
P0, P1, P2, P3: protection byte (see Table 8-2)

Table 8-2 The fourth byte XY value

MSBLSB								XY16 hex
1	F	V	H	P3	P2	P1	P0	
1	0	0	0	0	0	0	0	80
1	0	0	1	1	1	0	1	9D
1	0	1	0	1	0	1	1	AB
1	0	1	1	0	1	1	0	B6
1	1	0	0	0	1	1	1	C7
1	1	0	1	1	0	1	0	DA
1	1	1	0	1	1	0	0	EC
1	1	1	1	0	0	0	1	F1

8.3 Register Description

The configuration of the configuration register of base address of frame buffer DMA_ADDRi_CONFIG (i=0,...,3) is defined as follows:

Register name	Address	Read / Write (R / W)	Function description	Reset value
DMA_ADDR0_CONFIG	0x1c280000	R/W	Frame buffer base address 0	32'h0
DMA_ADDR1_CONFIG	0x1c280008	R/W	Frame buffer base address 1	32'h0
DMA_ADDR2_CONFIG	0x1c280010	R/W	Frame buffer base address 2	32'h0
DMA_ADDR3_CONFIG	0x1c280018	R/W	Frame buffer base address 3	32'h0

DMA_ADDRi_CONFIG	Bit	Default values	Description
Frame buffer base address	31:0	32'h0	The software allocates the base address of four buffers, and the hardware places 4 fame data from address 0 to address 3, and then address 0 circularly. Each buffer size as a frame image size. It's used for DMA to read data and adopts the physical address.

The configuration of video pixel configuration register CAMIF_CONFIG_PIX is defined as follows. Therein, except 640x480 and 320x240, the rest video resolution needs to be defined by the configuration of CAMIF_CONFIG_PIX register.

Register name	Address	Read / Write (R / W)	Function description	Reset value
CAMIF_CONFIG_PIX	0xbc280020	R/W	Video resolution configuration register	32'h0

CAMIF_CONFIG_PIX	Bit	Default values	Description
Floating pixel resolution line number y	23:12	12'h0	For example, for the pixels of 1280x720, the pixel line number is configured to 720.
Floating pixel resolution column number x	11:0	12'h0	For example, for the pixels of 1280x720, the pixel column number is configured to 1280.

U and V base address configuration register (CAMIF_CONFIG_UOFFSET and CAMIF_CONFIG_VOFFSET) is defined as follows. The video resolution except 640x480 and 320x240, the configuration buffer needs to specify the storage base address of U and V components in frame buffer in the format of YUV4:2:2 through base address configuration register. However, in RGB output display, the offset of CAMIF_CONFIG_UOFFSET configuration array display address is namely the address interval between lines in an image. For example, the 640x480 image is displayed in 1280x720 screen, and there are uoffset=(1280-640)x pixel bytes.

Register name	Address	Read / Write (R / W)	Function description	Reset value
CAMIF_CONFIG_UOFFSET	0xbc280028	R/W	U base address	32'h0
CAMIF_CONFIG_VOFFSET	0xbc280030	R/W	V base address	32'h0

CAMIF_CONFIG_UOFFSET	Bit	Default values	Description
U base address configuration register	31:0	32'h0	1/2 of frame buffer in the format of YUV4:2:2 is u component Base address. For example, in 1280x720 resolution, voffset is decimal 1280x720, and the unit is byte.
CAMIF_CONFIG_VOFFSET	**Bit**	**Default values**	**Description**
V base address configuration register	31:0	32'h0	3/4 of frame buffer in the format of YUV4:2:2 is u component Base address. For example, in 1280x720 resolution, voffset is decimal 1280x720 x3/2, and the unit is byte.

CAMIF_CONFIG configuration is the control register of starting and closing camera module, and is defined as follows:

Register name	Address	Read /	Function	Reset value

		Write (R / W)	description	
CAMIF_CONFIG	0xbc280038	R/W	Status register	32'h0

CAMIF_CONFIG	Bit	Default values	Description
CONFIG_PARA_CLR	31:31	1'b0	1: Start CAMERA 0: Close CAMERA
CONFIG_BUF_FULL	23:20	4'b0	Four frame buffers from low to high 1: filled 0: never written or writing
CONFIG_PARA_H_WD	19:16	4'b0	Wait valid Hsync delay beats
CONFIG_PARA_OUTPUT_D ATA_MODE	14:13	2'b0	0: YUV422 1: RGB565 2: RGB888 3: RGB0888
CONFIG_PARA_INPUT_DAT A_MODE	12:11	2'b0	0: RGB 1: ITU-R BT.601 2: ITU-R BT.656
CONFIG_PARA_SCALE_MO DE	10:9	2'b0	0: no scaling 1: zoom out by one time. When the pixel is configurable, it's configured to 0.
CONFIG_PARA_640X480	8:7	2'b0	0: 320x240 1: 640x480 2: Configurable pixels
CONFIG_PARA_SINGLEFIE LDEN	6:6	1'b0	1: Single field 0: Non-single field (frame mode with 0)
CONFIG_PARA_YUV_ORDE R	5:4	2'b0	Permutation format of YUV422 0: YCbYCr 1: YCrYCb 2: CrYCbY 3: CbYCrY
CONFIG_PARA_BGR_EN	3:3	1'b0	1: RGB is arranged as BGR 0: RGB is arranged as RGB (the conversion of ITU-R BT.601/656 into RGB is effective)
CONFIG_PARA_RGB_FORM AT	2:2	1'b0	0: Input format of RGB is 565 1: Input format of RGB is 888
CONFIG_PARA_HS	1:1	1'b0	1: HSYNC active low 0: HSYNC active high
CONFIG_PARA_VS	0:0	1'b0	1: VSYNC low active 0: VSYNC high active

Notes: when the input format is ITU-R BT.656, Config_para_hs, Config_para_vs is only configured to 0.

8.4 Configuration Operations

8.4.1 Memory Accessing Mode

Output data of Camera interface controller, and its frame memory hierarchy is as follows:
The frame memory of CAMIF output consists of four cyclic memory spaces. For YCbCr output, each memory space consists of three memory spaces: brightness Y, chroma Cb and Cr. The start address of yuv3 component storage correspond to base address, 1/2 address and 3/4 address in space; for RGB output, each memory space stores each RGB pixel in sequence.
The storage mode of output data of Camera interface controller in memory is as follows: Storage mode of little endian is adopted in frame storage. AXI bus width is 64-bit. When the output is in the format of YCbCr, each Y or Cb or Cr has one byte, and is arranged in each corresponding area of frame address; when the output is RGB565, each pixel has two bytes; when the output is RGB888 (32bits), each pixel has four bytes; when the output is

RGB888 (24bits), each pixel has three bytes. As is shown in Figure 8-4.

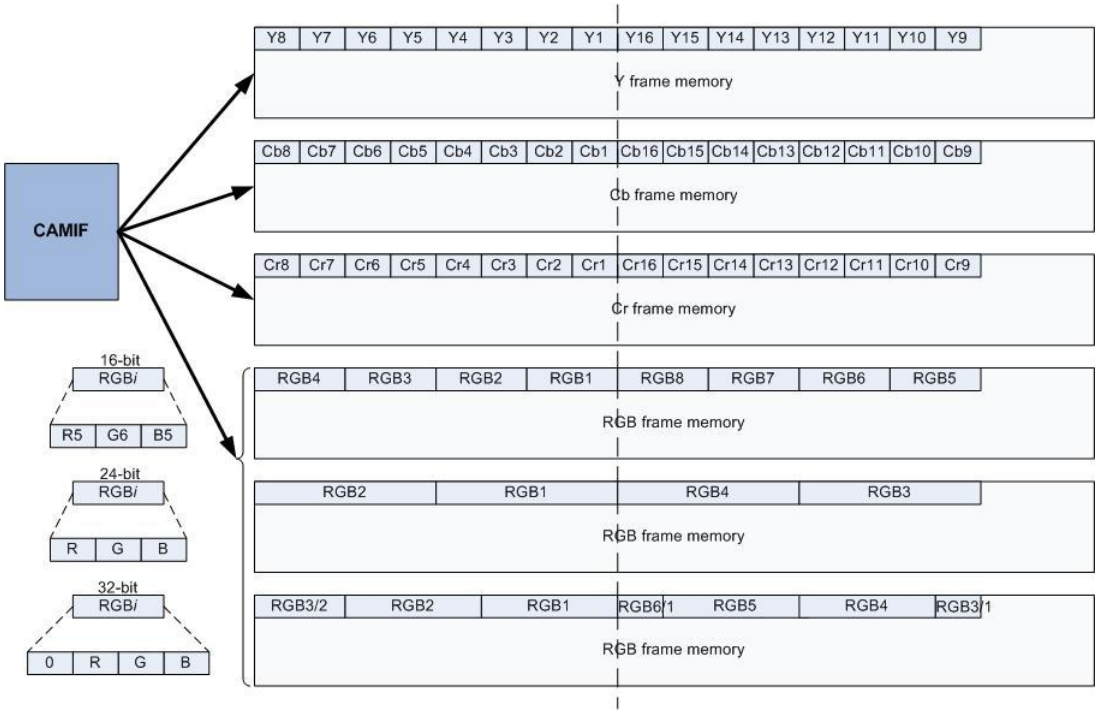

Figure 8-4 Storage mode

8.4.2 Configuration order

Before operation, CAMERA interface needs to configure some registers based on different conversion modes, and after the system reset, the register is default value. Only after the register configuration, can the module work. The working procedures of configuring CAMERA interface are as follows:

1. Read the status register message of Camera interface and obtain the 30th bit. When the bit is 1, it indicates the inside DMA is under idle status, and the following work configurations can be conducted. It's because DMA needs to interact with memory, and when we control the CAMERA interface work and stop, DMA can't stop in real time.
2. In working configuration, the base addresses of four address spaces to be stored are configured first. If for any pixel configuration and the output of YUV format, U and V addresses are required. Finally, the status register is configured, and its 31st bit is configured to 1, and then it can start work.
3. During work, CAMERA interface will send an interrupt to CPU after filling out one frame address space or covering the data in DMA module buffer. After the software receives the interrupt, the 23-20 and 28bit of status register can be inquired. The above 5 bits are all 0 in booting Camera interface, and then become 1 from high to low after filling out 23-20bits of one frame address space. When filling out one frame address space, the bit corresponding to the space becomes 0, and the software can query the status register to judge the storage of frame address space. When the data is covered, 28bit will be set to 1.
4. When the software wants to stop the operation of Camera interface, the 31st bit of the status register needs writing to 1. Under such circumstance, the Camera interface will stop analyzing the input in Camera, and DMA will stop sending any data to frame address space. After receiving all sent request responses, the 30th bit of the status register is set to 1.
5. When the application software of Camera interface is interrupted by other interrupts, the configuration request of closing Camera interface is added to interrupt hander. Restart it after waiting for recovery (firstly, the 31st bit of the status register is written to 0, and then 30th value is read. When the bit is 1, 1 is written to the 29th bit. And then the 30th bit is read, when the bit is 0, 1 is written to the 31st bit). Don't close Camera interface, and judge the stored information of frame address space and accept or reject the image based on the information of status register.

9 I2S Controller

9.1 Overview

Via APB interface, the data width of I2S controller in 1C is 32 bits, and it supports DMA transmission and several companies'! codec chip. I2S controller only supports the master mode, and I2S generates bit clock signal and left and right sound channel selection clock signal.

I2S features include:

- It supports the audio data sampling bit width of 8, 16, 20, 24 and 32.
- It supports the left and right sound channel processing word width of 8, 16, 20, 24 and 32.
- It includes two buffer FIFOs, and the buffer capacity of FIFO is 8 bytes.
- The interrupt processing mode of I2S is configurable, and after I2S transmit and receiver interrupt functions are enabled, if it needs to write when the buffer fifo of two channel is full, and or it needs to read when the buffer fifo is empty, send the interrupt signal to CPU.
- I2S can provide the system clock for codec chip and the clock frequency is configurable. Interface block diagram of the module:

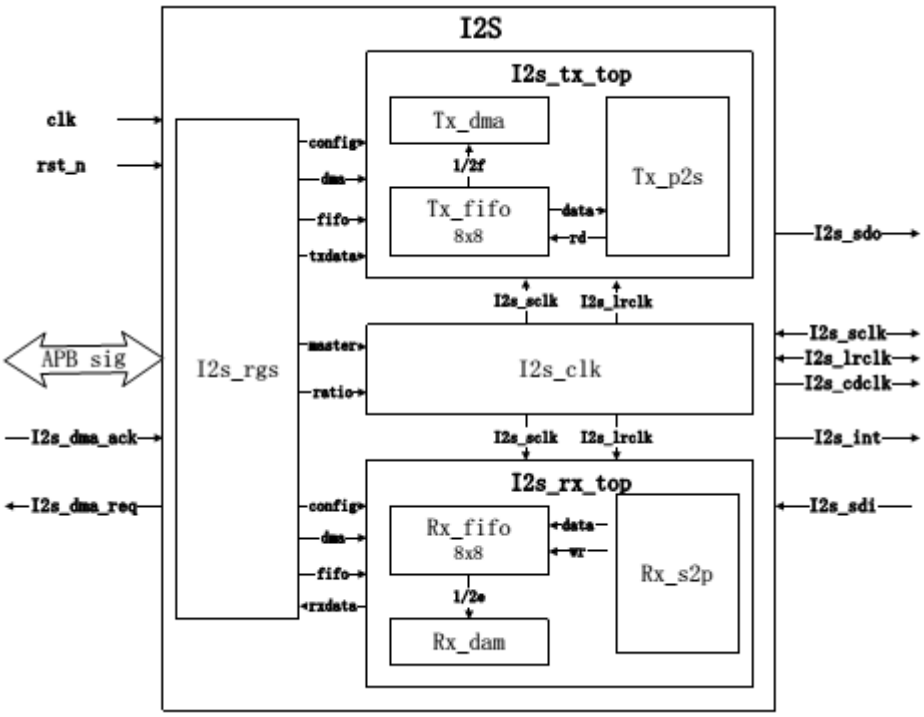

Figure 9-1 I2S interface block diagram

9.2 Interface Protocol

The operating time sequence of I2S receiver and transmitter is shown in Figure 9-2. The transmit operation sequential routine in the format of I2S of the receiver and transmitter is that the next frame data are transmitted in the 2nd bit clock after the signal selection signal changes, and the data transmits MSB bit first and then LSB bit. The bit width processed by receiver and transmitter may be inconsistent, and if the bit width of the data transmitted by transmitter is shorter than that of the supported data, LSB fill zero and send them. Or, some LSB data may be ignored; similarly, for receiver, when the bit width of the received data is smaller than that processed by it, LSB will fill zero and send them. Or, some LSB data may be ignored. Thus, for the received data, MSB is fixed, but LSB depends on the word length of the data to be received and transmitted, and the word length bit width configured by system.

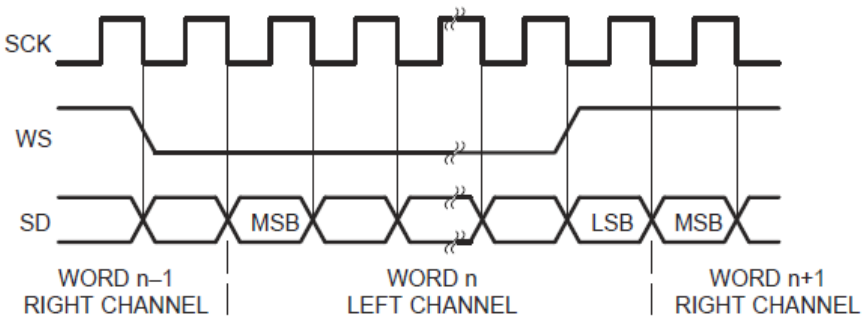

Figure 9-2 I2S transmission protocol

9.3 Dedicated Register

I2S includes five registers, and is as defined by the figure below.

Register name	Address	Read / Write (R / W)	Function description	Reset value
IISVersion	0xbfe6_0000	R/W	I2S identify register	32'h0
IISConfig	0xbfe6_0004	R/W	I2S configuration register	32'h0
IISControl	0xbfe6_0008	R/W	I2S control register	32'h0
IISRxData	0xbfe6_000c	R/W	I2S receive data register (used for DMA receive data)	32'h0
IISTxData	0xbfe6_0010	R/W	I2S transmit data register (used for DMA send data)	32'h0

The receive flag register allows the main control computer to read relevant operation information of the receiver. It identifies the address bit width of IIS, data bit width and version number.

IISVersion	Bit	Default values	Description
ADRW	9:8	2'h0	Address bus width: 00: Address width 8-bit 01: Address width 16-bit 10: Address width 32-bit 11: Address width 64-bit
DATW	5:4	2'h0	Data width 00: Address width 8-bit 01: Address width 16-bit 10: Address width 32-bit 11: Address width 64-bit
VER	3:0	4'h0	I2S version number

The receive configuration register configures the sound channel word length of I2S, the sampling depth of video data, and frequency division factor of each clock.

IISConfig	Bit	Default values	Description
LR_LEN	31:24	'h0	Word length handled by left and right sound tracks.

RES_DEPTH	23:16	'h0	Sampling depth settings: IIS sampling data length, effective scope of 8-32. If the transmitted or received data width is smaller than sampling data length, 0 is filled to low bit; if the transmitted or received data width is larger than sampling data length, the low bit is ignored.
SCLK_RATIO	15:8	'h0	Bit clock (BCLK) frequency coefficient: Bit clock frequency division factor, frequency division number is the bus clock frequency divided by 2x(RATIO+1)
MCLK_RATIO	7:0	'h0	System clock (MCLK) frequency division factor, system clock frequency division factor. The frequency division number is the bus clock frequency divided by 2x(RATIO+1)

The control register is used to configure the operation enable signal of IIS, buffer the store status of FIFO and relevant information state of information.

IISControl	Bit	Default values	Description
MASTER	15	'h0	1: IIS working in master mode
MSB LSB	14	'h0	1: High-order on the left end 0: High-order on the right end
RX_EN	13	'h0	When the bit of controller receive enable is 1, it's effective and starts to receive data.
TX_EN	12	'h0	When the bit of controller transmit enable is 1, it's effective and starts to transmit data.
RX_DMA_EN	11	'h0	DMA receiver enable, valid at 1
Reserved	10: 8	'h0	
TX_DMA_EN	7	'h0	DMA transmitter enable, valid at 1
Reserved	6:2	'h0	
RX_INT_EN	1	'h0	When the bit of RX interrupt enable is 1, it's enable interrupt. And when the bit is 0, it's forbidden.
TX_INT_EN	0	'h0	When the bit of TX interrupt enable is 1, it's enable interrupt. And when the bit is 0, it's forbidden.

9.4 Configuration Operations

For the normal operation of I2S, it's necessary to firstly configure CODEC chip, and then configuration register and control register of I2S controller.

1C chip communicates through I2C interface and CODEC chip. For CODEC chip as the slave device in I2C bus, detailed address, register and configuration method, please refer to the data manual of CODEC chip. After the configuration of CODEC, it's necessary to configure I2S controller. Some configuration messages are written to label register (I2SVersion) for search. First configure I2SConfig register, and then I2SControl register.

I2Sconfig register suggests that the configuration of LR_LEN and RES_DEPTH is the same, to avoid lost data or empty data during transmission. Based on the sampling frequency, sampling depth and frequency multiplying factor of CODEC, BCK clock is calculated via the formula below:

BCK = 256xfs (or 512xfs) or (768xfs); (see CODEC manual recommended configuration in details)

BCK_RATIO= Freq_SDRAM / (256 x fs) /2-1;

The computational formula is as follows if in dual-channel:

SCK = RES_DEPTH x 2 xfs;

SCK_RATIO= Freq_SDRAM / (RES_DEPTH x 2 x fs) /2 – 1;

Wherein fs is the configured sampling frequency. In transmitting and reading data, DMA is configured first and then controller to avoid lost data. See Section 14.3 for the configuration method of DMA multiplexing

10 Display Controller (DC)

10.1 Overview

Display controller fetches the frame buffer output from memory to external display interface.
The characteristics supported by display controller of Loongson 1C include:

- One-way DVI display, it supports 1024x768@60Hz at most.
- Five data formats: RGB444, RGB555, RGB565, RGB888, RGB8888
- Output dithering and gamma correction

10.2 Register Definition and Description

10.2.1 Frame buffer configuration register

Register name	Address	R/W	Description	Reset value
frameBufferConfi g	0xbc30_1240	R/W	Frame buffer configuration register	32'h0
frameBufferConfi g	bit	Description		Initial value
Reset	20	Soft reset when the value is changed into 0 from 1		0
Gamma	12	Write 1 enable gamma correction		0
Output Enable	8	Write 1 enable display output		0
Format	2:0	Color depth format: 0: none 1: RGB444 2: RGB555 3: RGB565 4: RGB888 5: RGB8888		0

10.2.2 Frame buffer address register 0

Register name	Address	R/W	Description	Reset value
frameBufferAddr0	0xbc301260	R/W	Frame buffer address register 0	32'h0
frameBufferAddr0	bit	Description		Initial value
Address	31:0	Physical address of buffer 0 in memory		0

10.2.3 Frame buffer address register 1

Register name	Address	R/W	Description	Reset value
frameBufferAddr1	0xbfe51580	R/W	Frame buffer address register 1	32'h0
frameBufferAddr1	bit	Description		Initial value
Address	31:0	The physical address of buffer 1 in memory (it needs to be the same with frame buffer address register 0)		0

10.2.4 Frame buffer span register

Register name	Address	R/W	Description	Reset value
frameBufferStride	0xbc301280	R/W	Frame buffer span register	32'h0
frameBufferStride	bit	Description		Initial value
Stride	31:0	Display the number of bytes in buffer line. When the format of RGB888 (24bit) is used, stride needs to round up to an integer based on 120 bytes. When the format of RGB8888 (32bit) is used,		0

		stride needs to round up to an integer based on 128 bytes.	

10.2.5 Color dithering configuration register

Register name	Address	R/W	Description	Reset value
ditherConfig	0xbc301360	R/W	Color dithering configuration register	32'h0
ditherConfig	bit	Description		Initial value
Enable	31	Write 1 enable color dithering function		0
RedSize	19:16	Red domain width		0
GreenSize	11:8	Green domain width		0
BlueSize	3:0	Blue domain width		0

10.2.6 Color vibrance lookup table low-bit register

Register name	Address	R/W	Description	Reset value
ditherTableLow	0xbc301380	R/W	Color dithering lookup table low-bit register	32'h0
ditherTableLow	bit	Description		Initial value
Y1_X3	31:28	Comparison value at coordinate (3,1)		0
Y1_X2	27:24	Comparison value at coordinate (2.1)		0
Y1_X1	23:20	Comparison value at coordinate (1.1)		0
Y1_X0	19:16	Comparison value at coordinate (0.1)		0
Y0_X3	15:12	Comparison value at coordinate (3.0)		0
Y0_X2	11:8	Comparison value at coordinate (2.0)		0
Y0_X1	7:4	Comparison value at coordinate (1.0)		0
Y0_X0	3:0	Comparison value at coordinate (0.0)		0

10.2.7 Color dithering lookup table high-bit register

Register name	Address	R/W	Description	Reset value
ditherTableHigh	0xbc3013a0	R/W	Color dithering lookup table high-bit register	32'h0
ditherTableLow	bit	Description		Initial value
Y3_X3	31:28	Comparison value at coordinate (3.3)		0
Y3_X2	27:24	Comparison value at coordinate (2.3)		0
Y3_X1	23:20	Comparison value at coordinate (1.3)		0
Y3_X0	19:16	Comparison value at coordinate (0.3)		0
Y2_X3	15:12	Comparison value at coordinate (3.2)		0
Y2_X2	11:8	Comparison value at coordinate (2.2)		0
Y2_X1	7:4	Comparison value at coordinate (1.2)		0
Y2_X0	3:0	Comparison value at coordinate (0.2)		0

10.2.8 Color dithering description

The function of color dithering is used to enhance the pixel value based on certain rules. In the below example, the implementation procedures of color dithering function will be explained.

Firstly, to determine which data to enhance (namely, 1 is added to the data bit), and it's necessary to configure register Display Dither Configuration. For example, the configuration RedSize is 6 (between 1 and 8, including 1 and 8), it indicates enhancing the 6^{th} bit in MSB bit, namely, the RedColor[2] of RedColor[7:0] is enhanced. It's also true of GreenSize and BlueSize.

Secondly, it's necessary to build the lookup table, namely, configuration register Display Dither Table. The lookup table includes 16 items, namely, 16 thresholds, and four bit width for each item.

The lookup table is indexed through the lowest 2 bits x[1:0] of x-coordinate and the lowest 2 bits y[1:0] of y-coordinate of screen pixel counter, and one threshold U[3:0] is obtained.

The lowest four bits of the pixel corresponding to screen (x, y) location is compared with the found threshold. If RedColor[3:0] > U[3:0] and RedColor[7:2] isn't 6 'b111111, 1 is added to RedColor[2] bit, and the color is enhanced.

10.2.9 LCD panel configuration register

Register name	Address	R/W	Description	Reset value
panelConfig	0xbc3013c0	R/W	LCD panel configuration register	32'h101
panelConfig	bit	Description		Initial value
ClockPol	9	Clock polarity, write 1 negation		0
ClockEn	8	Clock enable, write 1 enable		1
DEPol	1	Data enable polarity, write 1 negation		0
DE	0	Data enable, write 1 enable		1

10.2.10 Horizontal display width register

Register name	Address	R/W	Description	Reset value
HDisplay	0xbc3014a0	R/W	Horizontal display width register	32'h0
HDisplay	bit	Description		Initial value
Total	27:16	Total pixel number of one display line (including non-display area)		0
Display	11:0	The number of pixels in the display area of the display screen line		0

10.2.11 Line synchronization configuration register

Register name	Address	R/W	Description	Reset value
HSync	0xbc301400	R/W	Line synchronization configuration register	32'h40000000
HSync	bit	Description		Initial value
Pol	31	Line synchronization polarity, write 1 negation		0
Pulse	30	Line synchronization enable, write 1 enable		1
End	27:16	The number of pixels at the end of the line synchronization		0
Start	11:0	The number of pixels at the start of the line synchronization		0

10.2.12 Vertical display height register

Register name	Address	R/W	Description	Reset value
VDisplay	0xbc301480	R/W	Vertical display height register	32'h0
VDisplay	bit	Description		Initial value
Total	26:16	total pixel number of one display column (including non-display area)		0
Display	10:0	The number of pixels in the display area of the display screen column		0

10.2.13 Field synchronization configuration register

Register name	Address	R/W	Description	Reset value
VSync	0xbc3014a0	R/W	Field synchronization configuration register	32'h40000000
VSync	bit	Description		Initial value
Pol	31	Field synchronization polarity, write 1 negation		0
Pulse	30	Field synchronization enable, write 1 enable		1

End	26:16	The number of pixels at the end of the field synchronization	0
Start	10:0	The number of pixels at the start of the field synchronization	0

10.2.14 Output sequencing

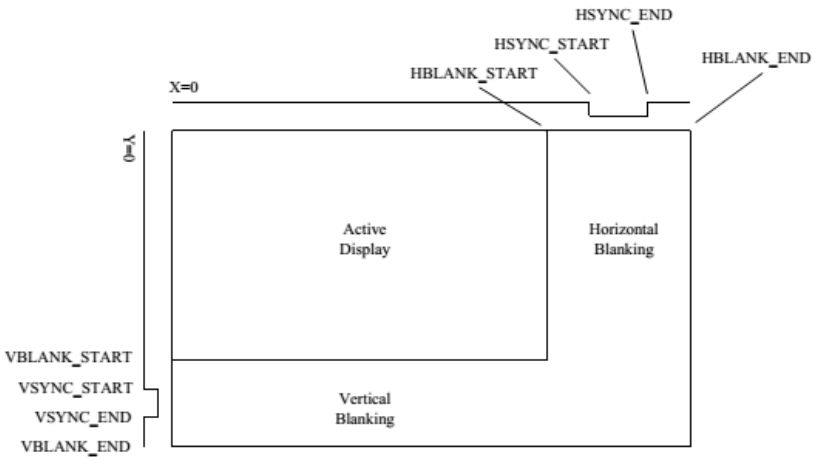

Figure 10-1 Display controller output sequencing

10.2.15 Gamma correction catalog register

Register name	Address	R/W	Description	Reset value
GammaIndex	0xbc3014a0	R/W	Gamma correction catalog register	32'h0
GammaIndex	bit	Description		Initial value
Index	7:0	It indicates Gamma adjustment from which option in color values of 0-255, and it's generally set to 0. It's only configured one time, and later the hardware will automatically increase the value.		0

10.2.16 Gamma correction value register

Register name	Address	R/W	Description	Reset value
GammaData	0xbc301500	R/W	Gamma correction value register	32'h0
GammaIndex	bit	Description		Initial value
Red	23:16	The red area of Gamma adjustment. The value indicated by Gamma Index is adjusted to the value of the current domain		0
Green	15:8	The green area of Gamma adjustment. The value indicated by Gamma Index is adjusted to the value of the current domain		0
Blue	7:0	The blue area of Gamma adjustment. The value indicated by Gamma Index is adjusted to the value of the current domain		0

10.2.17 Gamma correction instructions

The Gamma adjustment module includes three lookup tables, one responsible for red, one for green, and one for blue.

Lookup table can be rewritten by register. Lookup table can only be written.

One Gamma adjustment is as follows: (primary color, adjustment color) In the setup of Gamma color lookup table, the register should be configured in the sequence of color value.

Firstly, configure register Gamma Index to 0, indicating that the gamma adjustment starts from 0, and then the Gamma Data register is configured 256 times to complete the configuration: 0, 2, 5, 6……

11 MAC Controller

11.1 DMA Register Description

Loongson 1C has integrated one MAC controller. The DMA controller integrated inside MAC cooperates with MAC data transmission; this DMA controller can't be used by other modules, and MAC can't use other external DMAs. MAC controller register include MAC register and DMA register. The start address of MAC register is 0xbfe1_0000, and that of DMA register is 0xbfe1_1000.
The significance of DMA register and MAC register is introduced in the below.

11.1.1 Register0 (Bus Mode Register)

Parameter name	Bit	Default values	Description
Register0 (Bus Mode Register) Offset: 0x00			
Reserved	31:27	0x0	Reserved, read only
MB: Mixed Burst	26	0x0	When the bit is high, and FB bit is low, AXI master adopts the INCR access mode when the burst access length is longer than 16bit, and adopts the FIX access mode when the burst access length is or shorter than 16. Users need not care about this bit setting.
AAL: Address-Aligned Beats	25	0x0	When this bit and FB bit are both high, all accesses of AXI interface will be aligned to LS bit of the initial address. If FB bit is 0, the initial access address isn't aligned, and the rest is aligned. Users need not care about this bit setting.
8XPBL Mode If enable PBLX8 mode	24	0x0	When the bit is high, the maximum burst data transmission length of MAC DMA is 8,16,32,64,128 or 256. The maximum burst length depends upon PBL. Users need not care about this bit setting.
USP:Use Separate PBL	23	0x0	When this bit is high, PBL value only applies to TxDMA. When this bit is low, PBL value only applies to TxDMA and RxDMA. Users need not care about this bit setting.
RPBL: RxDMA PBL RxDMA burst transmission length	22:17	0x01	It indicates the maximum burst transmission length in the first RxDMA transmission. Can only be 1, 2, 4, 8, 16 and 32, and other values are ineffective.
FB Fixed Burst Fixed-length burst transfer length enable	16	0x0	It assigns whether AXI Master interface adopts FIX burst transmission mode. Users need not care about this bit setting.
PR: Rx:Tx priority ratio	15:14	0x0	Effective when DA bit is 0. 00: 1: 1 01: 2: 1 10: 3: 1 11: 4: 1
PBL: Programmable Burst Length	13:8	0x21	Users need not care about this setting.

ATDS: Alternate Descriptor size Whether to use 32 bytes size descriptor	7	0x0	When the bit is 1, the 32-byte descriptor is used. When the bit is 0, the 16-byte descriptor is used.
DSL: Descriptor Skip Length	6:2	0x00	Set 2 descriptor distances When the value is 0, it's the size of DMA descriptor by default.
DA:DMA Arbitration scheme	1	0x0	0: adopt the alternative arbitration mechanism between RxDMA and TxDMA 1: 1: RxDMA priority is higher than TxDMA priority See specific ratio for PR value.
SWR:Software Reset	0	0x21	If this bit is set high, DMA controller will reset MAC internal register and logic. The bit is automatically cleared when reset is finished.

11.1.2 Register2 (Receive Poll Demand Register)

Register1 (Transmit Poll Demand Register)Offset: 0x04			
TPD: Transmit Poll Demand	31:0	0x0	Write any value to this value, sending DMA controller will read the descriptor corresponding to register 18. If the descriptor is invalid, DMA transmission will terminate. If the descriptor is valid, DMA transmission will continue.

11.1.3 Register2 (Receive Poll Demand Register)

Register2 (Receive Poll Demand Register) 0x08			
RPBL: Receive Poll Demand	31:0	0x0	Write any value to this value, receiving DMA controller will read the descriptor corresponding to register 18. If the descriptor is invalid, DMA transmission will terminate. If the descriptor is valid, DMA transmission will continue.

11.1.4 Register3 (Receive Descriptor List Address Register)

Register3 (Receive Descriptor List Address Register)Offset: 0x0C			
Start of Receive List	31:0	0x0	Starting address of directional reception descriptor

11.1.5 Register4 (Transmit Descriptor List Address Register)

Register4 (Transmit Descriptor List Address Register)Offset: 0x10			
Start of Transmit List	31:0	0x0	Starting address of directional transmission descriptor

11.1.6 Register5 (Status Register)

Register5 (Status Register) Offset: 0x14			
Reserved	31:30		Reserved, read only
TTI: Time-Stamp Trigge Interrupt	29	0x0	Timestamp module triggering an interrupt. Read only.
GPI: MAC PMT	28	0x0	Power supply management module triggering an interrupt. Read only.

Interrupt			
GMI:MAC MMC Interrupt	27	0x0	MMC module triggering an interrupt. Read only.
GLI: MAC Line interface Interrupt	26	0x0	MAC module PCS or RGMII module trigger interrupt Read only
EB: Error Bits	25:23	0x0	23: 1'b1 TxDMA error during data transmission 1'b0 RxDMA error during data transmission
			24:1 'b1 reading transmission error 1'b0 writing transmission error 25:1 'b1 descriptor access error 1'b0 data cache access error
TS: Transmit Process State	22:20	0x0	3'b000: transmit stop; reset or stop command transmitting 3'b001: in progress; obtain transmit descriptor 3'b010: in progress; status of waiting for transmission 3'b011: in progress; read data from transmitting buffer, and send to transmit FIFO (TxFIFO) 3'b100: write-in timestamp status 3'b10-1: reserved 3'b110: suspended; the traditional descriptor can't be used for the transmit buffer underflows 3'b111: operation; close transmit descriptor.
RS: Receive Process State	19:17	0x0	3'b000: stop; reset or receive the stop command 3'b001: operation; obtain the receive descriptor 3'b010: reserved 3'b011: run; waiting to receive the package. 3'b100: pause; receive descriptor unavailable; 3'b101: operation; close the receive descriptor. 3'b110: timestamp writing status. 3'b111: operation; transfer the receive buffer from package content to system memory
NIS: Normal Interrupt Summary	16	0x0	Prompt system if there is a normal interrupt.
AIS: Abnormal Interrupt Summary	15	0x0	Prompt system if there is a normal interrupt.
ERI: Early Receive Interrupt Receive	14	0x0	Prompt: DMA controller write the first data in package to receive buffer
FBI: Fatal Bus Error Interrupt	13	0x0	Prompt bus error. See [25:23] for specific information. When this bit is set DMA engine stopping bus access operation.
Reserved	12:11	0x0	Reserved

ETI: Early Transmit Interrupt	10	0x0	Prompt that the Ethernet frame to be transmitted has been completely transmitted to the transmit FIFO in MTL module
RWT: Receive Watchdog Timeout	9	0x0	Prompt that one over 2048-byte Ethernet frame is received (when the huge frame is enabled, it prompts that one over 10240bytes Ethernet frame has been received)
RPS: Receive Process Stopped	8	0x0	Indicate reception process stop
RU: Receive Buffer Unavailable	7	0x0	Indicate unavailable reception buffer
RI: Receive Interrupt	6	0x0	Indicate frame reception completion The status information received by frame has been written to the descriptor. Reception in running status
UNF: Transmit Underflow	5	0x0	Receive underflow exists in indicate frame transmission process
OVF: Receive Overflow	4	0x0	Receive overflow exists in indicate frame receive process
TJT:Transmit Jabber Timeout	3	0x0	
TU: Transmit Buffer Unavailable	2	0x0	It prompts that the next descriptor in transmission list can be accessed by DMA controller.
TPS: Transmit Process Stopped	1	0x0	Prompt transmission process stop
TI: Transmit Interrupt	0	0x0	Prompt the completion of frame transmission and the 31st bit set of the first descriptor

11.1.7 Register0 (Bus Mode Register)

Register6 (Operation Mode Register)Offset: 0x18			
Reserved	31:27	0x0	Reserved
DT Close and abandon the Ethernet frame with TCP/IP Checksum error	26	0x0	When the bit is 1, MAC won't abandon the Ethernet frame with checksum error
RSF: Receive Store and Forward	25	0x0	When the bit is 1, the MTL module only receively the Ethernet frame completely stored in the receive FIFO.
DFF: Disable Flushing of Received Frames	24	0x0	When the bit is 1, don't wash out any Ethernet frame if the receive DMA is unavailable in receive descriptor or buffer.
RFA[2]: MSB of Threshold for Activating Flow Control	23	0x0	100: maximum value minus 5KB 101: maximum value minus 6KB 110: maximum value minus 7KB 111: reserved (Note: a maximum value of 8KB)
RFD[2]: MSB of Threshold for	22	0x0	100: maximum value minus 5KB 101: maximum value minus 6KB

Deactivating Flow Control			110: maximum value minus 7KB 111: reserved (Note: a maximum value of 8KB)
TSF: Transmit Store and Forward	21	0x0	When the bit is 1, the content that the frame sends all enters in the transmit FIFO of MTL.
FTF:Flush Transmit FIFO	20	0x0	When the bit is 1, the transfer control logic is reset to the default, and will cause the sent data in FIFO to be completely lost.
Reserved	19:17	0x0	Reserved
TTC:Transmit Threshold Control	16:14	0x0	When the frame size exceeds this value, MTL will transmit this frame. 000: 64 bytes 001: 128 bytes 010: 192 bytes 011: 256 bytes 100: 40 bytes 101: 32 bytes 110: 24 bytes 111: 16 bytes
ST:Start/Stop Transmission Command	13	0x0	When this bit is 1, the transmission enters into the running state. When this bit is 0, the transmission enters into the halted state.
RFD:Threshold for deactivating flow control	12:11	0x0	00: Maximum value minus 1KB 01: Maximum value minus 2KB 10: Maximum value minus 3KB 11: Maximum value minus 4KB (Maximum value of 8KB)
RFA:Threshold for Activating flow control	10:9	0x0	00: Maximum value minus 1KB 01: Maximum value minus 2KB 10: Maximum value minus 3KB 11: Maximum value minus 4KB (Maximum value of 8KB)
EFC: Enable HW flow control	8	0x0	When the bit is 1, the hardware flow control circuit based on receive FIFO will be effective.
FEF:Forward Error Frames	7	0x0	When the bit is 1, the error frame is received (error frame includes CRC error collision error, Jumbo frame, Watchdog timeout, overflow, and the like.)
FUF:Forward Undersized Good Frames Receive error-free small frames	6	0x0	When the bit is 1, the receive FIFO will receive the Ethernet frame without error but smaller than 64 bytes.
Reserved	5	0x0	Reserved
RTC: Receive Threshold Control	4:3	0x0	The content that MTL transmits in receive FIFO has exceeded the set size. 00: 64 bytes 01:32 bytes 10: 96 bytes 11: 128 bytes
OSF: Operation Second Frame	2	0x0	When the bit is high, DMA can start to process the second Ethernet frame when the status of the first Ethernet frame has been written.
SR:Start/Stop Receive	1	0x0	When the bit is set high, the receiving enters into the running state. When the bit is set low, the receiving enters into the halted state.
Reserved	0	0x0	Reserved

11.1.8 Register7 (Interrupt Enable Register)

Register7 (Interrupt Enable Register)Offset: 0x1C			
Reserved	31:17	0x0	Reserved
NIE:Normal Interrupt Summary Enable	16	0x0	When the bit is 1: if the bit of the normal interrupt enable is 0: the normal interrupt disable
AIE: Abnormal Interrupt Summary Enable	15	0x0	When this bit is 1: abnormal interrupt enable. When this bit is 0: abnormal interrupt disable.
ERE: Early Receive Interrupt Enable	14	0x0	When this bit is high: early receive interrupt enable
FBE:Fatal Bus Error Enable	13	0x0	When the bit is high: bus fatal error interrupt enable
Reserved	12:11	0x0	Reserved
ETE: Early Transmit Interrupt Enable	10	0x0	When this bit is high: early enable transmission interrupt
RWE: Receive Watchdog Timeout Interrupt Enable	9	0x0	When this bit is high: enable receive watchdog timeout interrupt.
RIE: Receive Stopped Interrupt Enable	8	0x0	When this bit is high: enable receive stopped interrupt.
RUE: Receive Buffer Unavailable Interrupt Enable	7	0x0	When the bit is high, enable the receive buffer unavailable interrupt.
RIE: Receive Interrupt Enable	6	0x0	When this bit is high: enable receive interrupt.
UNE: Underflow Interrupt Enable Transmit FIFO underflow interrupt enable	5	0x0	When the bit is high: enable transmit FIFO underflow interrupt
OVE: Overflow Interrupt Enable Receive FIFO overflow interrupt enable	4	0x0	When the bit is high: enable receive FIFO overflow interrupt
TJE: Transmit JabberTimeout Enable	3	0x0	When the bit is high: enable Jabber timeout interrupt
TUE:Transmit Buffer Unavailable Enable	2	0x0	When the bit is high: enable transmit buffer unavailable interrupt
TSE: Transmit Stopped Enable	1	0x0	When this bit is high: enable transmit stopped interrupt.
TIE: Transmit Interrupt Enable	0	0x0	When this bit is high: enable transmission interrupt

11.1.9 Register8 (Missed Frame and Buffer Overflow Counter Register)

Register8 (Missed Frame and Buffer Overflow Counter Register)Offset: 0x02			
Reserved	31:29	0x0	Reserved
Overflow bitfor FIFO Overflow Counter	28	0x0	FIFO overflow indicating bit
Indicates the number of frames missed by the application	27:17	0x0	Indicate missing frame numbers of the application programs

Overflow bit for Missed Frame Counter	16	0x0	Indicates the number of missed frame has exceeded the maximum value
Indicates the number of frames missed by the controller due to the Host Receive Buffer being unavailable	15:0	0x0	Indicates the number of frames missed by the controller due to the Host Receive Buffer being unavailable

11.1.10 Register9(Receive Interrupt Watchdog Timer Register)

Register9(Receive Interrupt Watchdog Timer Register)Offset: 0x24			
Reserved	31:8	0x0	
RIWT: RI Watchdog Timer count	7:0	0x0	When the Watchdog is set, it indicates the count in the unit of the clock cycle x 256 When DMA receives the data packet, and the count starts when the RI bit in status register is 0, when the Watchdog timer times out, RI bit is set to 1. The domain resets when RI bit is 1

11.1.1 Register0 (Bus Mode Register)

Register10 (AXI Bus Mode Register)Offset: 0x28			
EN_LPI: Enable LPI (LowPower Interface)	31	0x0	When the bit is 1, the low power interface is enabled, and the system receives the LPI request from AXI system clock controller. When the bit is 0, the low power interface is disabled, and the system will refuse the LPI request forever.
UNLCK_ON_MGK_RWK:Unlock on Magic Packet or Remote Wake Up	30	0x0	When the bit is 1, if MAC is in low power state, it can return to the working state only by magic packet or remote wakeup; when the bit is 0, MAC is under low power state, it can return to the working state via any packet.
Reserved	29:23	0x0	
WR_OSR_LMT: AXI Maximum Write Outstanding Request Limit	22:20	0x0	This bit has set up the maximum outstanding request number sent by AXI interface write operation.
AXI maximum outstanding Write out request			
Reserved	19	0x0	
WR_OSR_LMT: AXI Maximum Read Outstanding Request Limit	18:16	0x0	This bit has set up the maximum outstanding request number sent by AXI interface read operation.
Reserved	15:13	0x0	
AXI_AAL: Address-Aligned Beats	12	0x0	This bit is only-read, and is the same with AAL bit 0.
Reserved	11:8	0x0	
BLEN256: AXI Burst Length 256	7	0x0	Only when AXI_BURST_LENGTH is configured to 256, can this bit be significant; when the bit is 1, it indicates that AXI supports the request of Burst length of 256; or, it'' be reserved.
BLEN256: AXI Burst	6	0x0	Only when AXI_BURST_LENGTH is configured to

Length 128			128, can this bit be significant; when the bit is 1, it indicates that AXI supports the request of Burst length of 128; or it is be reserved.
BLEN256: AXI Burst Length 64	5	0x0	Only when AXI_BURST_LENGTH is configured to 64, can this bit be significant; when the bit is 1, it indicates that AXI supports the request of Burst length of 64; or it will be reserved.
BLEN256: AXI Burst Length 32	4	0x0	Only when AXI_BURST_LENGTH is configured to 32, can this bit be significant; when the bit is 1, it indicates that AXI supports the request of Burst length of 32; or it will be reserved.
BLEN256: AXI Burst Length 16	3	0x0	Only when AXI_BURST_LENGTH is configured to 16, can this bit be significant; when the bit is 1, it indicates that AXI supports the request of Burst length of 16; or, it" be reserved.
BLEN256: AXI Burst Length 8	2	0x0	Only when AXI_BURST_LENGTH is configured to 8, can this bit be significant; when the bit is 1, it indicates that AXI supports the request of Burst length of 8; or it will be reserved.
BLEN256: AXI Burst Length 4	1	0x0	Only when AXI_BURST_LENGTH is configured to 4, can this bit be significant; when the bit is 1, it indicates that AXI supports the request of Burst length of 4; or, it" be reserved.
UNDEF: AXI Undefined Burst Length	0	0x0	When the bit is 1, it indicates that AXI interface can send the request of any Burst length. When the bit is 0, it indicates that AXI supports the request length that bit7-1 defines to be 256/128/64/32/16/8/4 or 1.

11.1.12 Register11 (AXI Status Register)

Register11 (AXI Status Register)Offset: 0x2C			
Reserved	31:2	0x0	
	1	0x0	When the bit is 1, it indicates that the current AXI is sending read request.
	0	0x0	When the bit is 1, it indicates that the current AXI is sending read request.

Register12- Register18: **Reserved**

11.1.13 Register18 (Current Host Transmit Descriptor Register)

Register18 (Current Host Transmit Descriptor Register)Offset: 0x48			
Host Transmit Descriptor Address Pointer	31:0	0x0	Read only

11.1.14 Register19 (Current Host Receive Descriptor Register)

Register19 (Current Host Receive Descriptor Register)Offset: 0x4C			
Host Receive Descriptor Address Pointer	31:0	0x0	Read only

11.1.15 Register20 (Current Host Transmit Buffer Address Register)

Register20 (Current Host Transmit Buffer Address Register)Offset: 0x05

Host Transmit Buffer Address Pointer	31:0	0x0	Read only

11.1.16 Register21 (Current Host Receive Buffer Address Register)

Register21 (Current Host Receive Buffer Address Register)Offset: 0x54			
Host Receive Buffer Address Pointer	31:0	0x0	Read only

11.2 MAC Controller Register Description

11.2.1 Register0 (MAC Configuration Register)

Parameter name	Bit	Default values	Scope	Description
Register0 (MAC Configuration Register) Offset: 0x0000				
Reserved	31:26	0x0	Reserved	
TCH: Transmit Configuration in RGMII	24	0x0	When the bit is high, it'll transmit messages such as duplex mode, link speed, link and link connection/disconnection to PHY through RGMII interface.	
WD: Watchdog Disable	23	0x0	When the bit is high, MAC will disable the watchdog timer in RxD, and can receive the Ethernet frame as large as 16384 bytes.	
JD: Jabber Disable	22	0x0	When the bit is high, MAC will close the Jabber timer during transmission, and can send the Ethernet frame as large as 16384 bytes.	
BE: Frame Burst Enable	21	0x0	When the bit is high, MAC enables the frame burst transmission mode.	
JE: Jumbo Frame Enable	20	0x0	When the bit is high, MAC enables the Jumbo frame receive (as large as 9018 bytes).	
IFG: Minimum Inter-Frame Gap	19:17	0x0	Set the minimum inter-frame gap during transmission process 000: 96 bit-time 001: 88 bit-time 010: 80 bit-time …. 111: 40 bit-time	
DCRS: Disable Carrier Sense During Transmission	16	0x0	When the bit is high, MAC will ignore the detection of CRS signal in half-duplex mode.	
PS: Port Select	15	0x0	0: GMII (1000Mbps) 1: MII(10/100Mbps)	
FES: Speed Fast Ethernet speed prompt	14	0x0	0: 10Mbps 1: 100Mbps	
DO: Disable Receive Own	13	0x0	When the bit is high, MAC doesn't receive the valid Ethernet frame of gmii_txen_o in half-duplex mode.	
LM: Loopback Mode	12	0x0	When the bit is high, GMII/MII works in loopback mode.	
DM: Duplex Mode	11	0x0	When the bit is high, MAC works in full-duplex mode,	

			and it can send and receive the Ethernet frame simultaneously in full-duplex mode.
IPC: Checksum Offload Enable	10	0x0	When the bit is high, MAC hardware computes the received payload of Ethernet frame. It also checks the checksum of IPV4 head
DR: Disable Retry	9	0x0	When the bit is high, when encountering the collision, MAC won't retransmit the Ethernet frame, and only report the collision error.
LUD: Link Up/Down	8	0x0	0: Link disconnect 1: Link connection
ACS: Automatic Ethernet frame Pad/CRC Stripping	7	0x0	When the bit is 1, MAC eliminates the Pad and FCS in the received Ethernet frame.
BL: Back-Off Limit	6:5	0x0	The back-off limit decides the slot-based delay time 00: k=min(n,10) 01: k=min(n,8) 10: k=min(n,4) 11: k=min(n,1)
DC Deferral Check	4	0x0	When the bit is 1, enable deferral detection function
TE: Transmitter Enable	3	0x0	When the bit is 1, enable MAC transfer function
RE: Receiver Enable	2	0x0	When the bit is 1, enable MAC receive function
Reserved	1:0	0x0	Reserved

11.2.2 Register1 (MAC Frame Filter)

Register1 (MAC Frame Filter)	Offset: 0x0004		
RA: Receive All	31	0x0	When the bit is 1, MAC receive module transmits all received frames to application, and ignore source address/target address filtering mechanism.
Reserved	30:11	0x0	Reserved
HPF: Hash or Perfect Filter	10	0x0	When the bit is 1, the Ethernet frame in Hashor Perfect Filter system is sent to application. When the bit is 0, only the Ethernet frame in Hashor Perfect Filter system is sent to application.
SAF: Source Address Filter Enable	9	0x0	MAC CORE compares the source address domain in the received Ethernet frame and the value in SA register, and if they are matching, the SAMatch bit in receive status register is set to high. When the bit is 1, the source address matching fails, and MAC CORE will lose the Ethernet frame. When the bit is 0, no matter whether the source address matching result receives MAC CORE, the matching result will be written to receive status register.
SAIF: SA Inverse Filtering	8	0x0	When the bit is 2, the Ethernet frame matching the source address in SA register will mark that the source address matching fails. When the bit is 0, the Ethernet frame mismatching the source address in SA register will mark that the source address matching fails.
PCF: Pass Control Frames	7:6	0x0	00: MAC filters all control frames 01: MAC receives all control frames except pause frame

			10: M AC receives all control frames. 11: MAC receives the control frame based on address filtering.
DBF: Disable Broadcast Frames	5	0x0	When the bit is 1, all received broadcast frames are filtered. Receive all broadcast frames when this bit is 0
PM: Pass All Multicast	4	0x0	Receive all multicast frames when this bit is 1 Filter all multicast frames when this bit is 0
DAIF: DA Inverse Filtering Target address inverse filtering	3	0x0	When the bit is 1, inverse target address matching is conducted for unicast and multicast When the bit is 0, inverse target address matching is conducted for unicast and multicast
HMC: Hash Multicast	2	0x0	When the bit is 1, the received multicast will conduct the target address filtering based on the contents in Hash table.
HUC: Hash Unicast	1	0x0	When the bit is 1, the received unicast will conduct the target address filter based on the contents in Hash table.
PR:Promiscuous Mode	0	0x0	Receive all Ethernet frames.

11.2.3 Register2 (Hash Table High Register)

Register2 (Hash Table High Register)	Offset: 0x0008		
HTH: Hash Table High	31:0	0x0	Hash Table High 32-bit

11.2.4 Register3 (Hash Table Low Register)

Register3 (Hash Table Low Register)	Offset: 0x0C		
HTL:HashTable Low	31:0	0x0	Hash Table Low 32-bit

11.2.5 Register4 (GMII Address Register)

Register4 (GMII Address Register)	Offset: 0x0010		
Reserved	31:16	0x0	Reserved
PA: Physical Layer Address	15:11	0x0	This domain chooses to assess which on in 32 PHYs.
GR GMII Register The register in PHY device to access	10:6	0x0	This domain chooses to access which GMII configuration register in PHY
Reserved	5	0x0	Reserved
CR:CSRClock Range	4:2	0x0	This domain decides whether MDC clock is clk_csr_i clock frequency ratio. 0000 clk_csr_i/42 0001 clk_csr_i/62 0010 clk_csr_i/16 0011 clk_csr_i/26 0100 clk_csr_i/102 0101 clk_csr_i/124 0110, 0111 Reserved
GW: GMII Write	1	0x0	When the bit is 1, write operation is conducted to PHY via GMII data register. When the bit is 0, read operation is conducted to PHY via GMII data register.

GB GMII Busy	0	0x0	Before the write operation in registers 4 and 5, this bit should be written to 0. Before the register 4 is written, this bit must be set to 0 first. When accessing to PHY register, the application needs to set the bit to 1, and it indicates that the write or read operation is under progress in GMII interface.

11.2.6 Register5 (GMII Data Register)

Register5 (GMII Data Register)Offset: 0x0014			
Reserved	31:16	0x0	Reserved
GD: GMII Data	15:0	0x0	This domain has saved 16 data in managing the read access or the write access of PHY.

11.2.7 Register6 (Flow Control Register)

Register6 (Flow Control Register)Offset: 0x0018			
PT: Pause Time	31:16	0x0	This field has saved the pause time domain in filling out transmission control frame.
Reserved	15:8	0x0	Reserved
DZPQ: Disable Zero-Quanta Pause	7	0x0	When the bit is 1, the generation of Zero-Quanta Pause is disabled
Reserved	6	0x0	Reserved
PLT: Pause Low Threshold	5:4	0x0	This domain is used to set the pause time threshold. 00: Pause time reduces 4 time slots 01: Pause time reduces 28 time slots 10: Pause time reduces 144 time slots 11: Pause time reduces 256 time slots (one time slot is the transmission time of 512bytes or 64bit in GMII/MII interface)
UP Unicast Pause Frame Detect	3	0x0	When the bit is 1, MAC will detect the pause based on the station unicast address
RFE: Receive Flow Control Enable	2	0x0	When the bit is 1, MAC will analyze the received stop frame, and pause the frame transmit based on the time specified by pause frame
TEF: Transmit Flow Control Enable	1	0x0	In full-duplex mode, when the bit is 1, MAC enables the transmission of pause frame. In half-duplex mode, when the bit is 1, MAC enables the backpressure operation.
FCB / BPA: Flow Control Busy/Backpressure Activate	0	0x0	When the bit is 1, in full-duplex mode, the pause frame is transmitted or in half-duplex mode, the backpressure operation is initiated.

11.2.8 Register7 (VLAN Tag Register)

Register7 (VLAN Tag Register)Offset: 0x1C			
Reserved	31:17	0x0	Reserved
ETV: Enable 12-Bit VLAN Tag Comparison	16	0x0	When the bit is 1, Enable 12-Bit VLAN Tag Comparison instead of 16-bit VLANTag to compare and filter Ethernet frames.
VL:VLAN Tag Identifier for Receive Frames	15:0	0x0	This domain saves the VLAN Tag in the format of 802.1Q, and uses it to compare the 15 and 16-bit VLAN Tag in the received Ethernet frame.

11.2.9 Register8 (Version Register)

Register8 (Version Register)Offset: 0x02			
Reserved	15:8	0x0	Reserved
Version	7:0	0x0	0X35

11.2.10 Register14 (Interrupt Status Register)

Register14 (Interrupt Status Register)Offset: 0x0038			
Reserved	15:8	0x0	Reserved
MMCReceive Checksum Offload Interrupt Status MMC	7	0x0	When the MMC Receive Checksum Offload register generates any interrupt, this bit is set to 1.
MMC Transmit Interrupt Status	6	0x0	When MMC transmit interrupt register generates any interrupt, this bit is set to 1.
MMCReceive Interrupt Status	5	0x0	When MMC receive interrupt register generates any interrupt, this bit is set to 1.
MMC InterruptStatus	4	0x0	When any bit of 7:5 is high, this bit is set to 1.
PMT Interrupt Status	3	0x0	In Power Down state, when the magic frame or Wake-on-LAN is received, this bit is set to 1.
PCS Auto-Negotiation	2	0x0	When the RGMII PHY interface finishes the negotiation automatically, this bit is set to 1.
PCS Link Status Changed	1	0x0	In the event of any change in the link status of RGMII PHY interface, this bit is set to 1.
RGMIIInterrupt Status	0	0x0	In the event of any change in the link status of RGMII interface, this bit is set to 1.

11.2.11 Register15 (Interrupt Mask Register)

Register15 (Interrupt Mask Register)Offset: 0x0C			
Reserved	15:10	0x0	Reserved
TimeStamp Interrupt Mask	9	0x0	When the bit is 1, the Time stamp interrupt is disabled.
Timestamp interrupt enable			
Reserved	8:4	0x0	Reserved
PMT Interrupt Mask	3	0x0	When the bit is 1, the interrupt caused on power management is disabled.
PCSAN Completion Interrupt Mask	2	0x0	When the bit is 1, PCS auto negotiation complete interrupt is disabled.
PCSLinkStatus Interrupt Mask	1	0x0	When the bit is 1, the interrupt caused by the change in PCS link status is disabled.
RGMIIInterrupt Mask	0	0x0	When the bit is 1, the interrupt caused by RGMII is disabled.

11.2.12 Register16 (MAC Address0 High Register)

Register16 (MAC Address0 High Register)Offset: 0x0040			
MO: Always 1 Reserved	31	0x0	Reserved
Reserved	30:16	0x0	Reserved
MAC	15:0	0x0	Store the MAC address used to receive address filtering

Address0[47:32] MAC address high 16-bit			and transmit flow control frame.

11.2.13 Register17 (MAC Address0 Low Register)

Register17 (MAC Address0 Low Register)	Offset: 0x0044		
MAC Address0[31:0] MAC address low 32-bit	31:0	0x0	Store the MAC address used to receive address filtering and transmit flow control frame.

11.2.14 Register18 (MAC Address1 High Register)

Register18 (MAC Address1 High Register)	Offset: 0x0048		
AE:Address Enable	31	0x0	When the bit is 1, the address filtering module uses the 2nd MAC address for complete address filtering. When the bit is 0, the address filter module doesn't use the 2nd MAC address for address filter.
SA:Source Address Source MAC address	30	0x0	When the bit is 1, MAC address 1 is used to compare the source MAC address of receive frame. When the bit is 0, MAC address 1 is used to compare the target MAC address of receiving frame.
MBC: Mask Byte Control	29:24	0x0	This domain is used to compare the byte mask control bit in each MAC address. For example, the 29th bit is used to mask [15:8] in mask register 18.
Reserved	23:16	0x0	Reserved
MAC Address1[47:32] The second MAC address high 16-bit	15:0	0xFFFF	

11.2.15 Register19 (MAC Address1 Low Register)

Register19 (MAC Address1 Low Register)	Offset: 0x0C		
MAC Address1[31:0] The second MAC address low 32-bit	31:0	0x0	

11.2.16 Register48 (AN Control Register)

Register48 (AN Control Register)	Offset: 0x0C		
Reserved	31:19	0x0	Reserved
SGMII RAL Control Reserved	18	0x0	Reserved
LR: Lock to Reference	17	0x0	When the bit is 1, PHY will lock its phase-locked loop to the 125MHz reference clock.
ECD: Enable Comma Detect	16	0x0	When the bit is 1, the pause detect and word resynchronization of PHY are enabled
Reserved	15	0x0	Reserved
ELE: External Loopback Enable	14	0x0	When the bit is 1, enable PHY enters into loopback mode.
Reserved	13	0x0	Reserved
ANE: Auto-Negotiation Enable	12	0x0	When the bit is 1, MAC will automatically negotiate with the link.
Reserved	11:10	0x0	Reserved
RAN: Restart Auto-Negotiation	9	0x0	When the bit is 1, the auto-negotiation restarts.
Reserved	8:0	0x0	Reserved

11.2.17 Register49 (AN Status Register)

Register49 (AN Status Register)Offset: 0x1c280018			
Reserved	31:9	0x0	Reserved
ES: Extended Status	8	0x0	It's only-read, because MAC supports the expansion state message.
Reserved	7:6	0x0	Reserved
ANC: Auto-Negotiation Complete	5	0x0	It's read-only, indicates that auto-negotiation is completed.
Reserved	4	0x0	Reserved
ANA: Auto-Negotiation Ability	3	0x0	It's only-read, because MAC supports the auto-negotiation.
LS: Link Status	2	0x0	When this bit is set to 1, indicating the link is connected. When this bit is 0, indicating the link is disconnected.
Reserved	1:0	0x0	Reserved

11.2.18 Register50 (Auto-Negotiation Advertisement Register)

Register50 (Auto-Negotiation Advertisement Register)Offset: 0x0C			
Reserved	31:16	0x0	Reserved
NP: Next Page Support	15	0x0	It's only read to 0, because MAC doesn't support the next page.
Reserved	14	0x0	Reserved
RFE: Remote Fault Encoding	13:12	0x0	When 2bit indicates the link opposite end is wrong, see subsection 37.2.1.5 in IEEE802.3z for specific codes.
Reserved	11:9	0x0	Reserved
PSE:Pause Encoding	8:7	0x0	See subsection 37.2.1.4 in IEEE802.3z
HD: Half-Duplex Half-duplex	6	0x0	When the bit is 1, it indicates MAC supports the half-duplex.
FD Full-Duplex	5	0x0	When the bit is 1, it indicates MAC supports the full-duplex.
Reserved	4:0	0x0	Reserved

11.2.19 Register51 (Auto-Negotiation Link Partner Ability Register)

Register51 (Auto-Negotiation Link Partner Ability Register)Offset: 0x1c280018			
Reserved	31:16	0x0	Reserved
NP: Next Page Support	15	0x0	When the bit is 1, it indicates more nexpage messages are available. When the bit is 0, it indicates the next page exchange is unavailable.
ACK: Acknowledge	14	0x0	It indicates that in auto-negotiation, the link opposite end successfully receives the basic page of MAC
RFE: Remote Fault Encoding	13:12	0x0	See subsection 37.2.1.5 in IEEE802.3z
Reserved	11:9	0x0	Reserved
PSE:Pause Encoding Opposite end pause status coding	8:7	0x0	See subsection 37.2.14 in IEEE802.3z
HD: Half-Duplex	6	0x0	Indicate that opposite end can be run in half-duplex mode.
FD Full-Duplex	5	0x0	Indicate that opposite end can be run in full-duplex mode.

Reserved	4:0	0x0	Reserved

11.2.20 Register52 (Auto-Negotiation Expansion Register)

Register52 (Auto-Negotiation Expansion Register)Offset: 0x0D			
Reserved	31:3	0x0	Reserved
NPA: Next Page Ability	2	0x0	It's only read to 0, because MAC doesn't support the next page.
NPR: New Page Received	1	0x0	When the bit is 1, it indicates that MAC receives the new page.
Reserved	0	0x0	Reserved

11.2.21 Register54 (SGMII/RGMII Status Register)

Register54 (SGMII/RGMII Status Register)Offset: 0x0D			
Reserved	31:4	0x0	Reserved
Link Status	3	0x0	When this bit is set to 1, indicating the link is connected. When this bit is set to 0, indicating the link is disconnected.
Link Speed	2:1	0x0	Indicate current link speed 00: 2.5MHz 01: 25MHz 10: 125MHz
Link Mode	0	0x0	0: Half-duplex 1: Full-duplex

IEEE1588 register:

11.2.22 Register448 (Time Stamp Control Register)

Register448 (Time Stamp Control Register)Offset: 0x0700			
Reserved	31:20	0x0	Reserved
ATSFC: Auxiliary SnapshotFIFO Clear	19	0x0	When the bit is 1, reset the pointer of Auxiliary Snapshot FIFO, clear FIFO. After this, the bit is 0.
TSENMACADDR: EnableMAC addressfor PTP frame filtering	18	0x0	When the bit is 1, the received PTP package will go through the MAC destination address filter (DA Fiter) in MAC, and the mismatching PTP packet will be abandoned.
TSCLKTYPE: Select the type of clock node	17:16	0x0	The domain is coded according to the following types: 00: Ordinary clock 01: Boundary clock 10: End-to-End Transparent clock 11: Peer-to-peer Transparent clock
TSMSTRENA: Enable Snapshot for Messages Relevant to Master	15	0x0	When the bit is 1, Snapshot records messages Relevant to Master; when the bit is 0, Snapshot records messages Relevant to Slave.

TSEVNTENA: Enable Time Stamp Snapshot for Event Messages	14	0x0	When the bit is 1, Snapshot only records the Event Message; when the bit is 0, Snapshot records all messages.
TSIPV4ENA: Enable TimeStamp Snapshot for IPv4 frames	13	0x0	When the bit is 1, the Time Stamp Snapshot of IPv4 frame is enabled.
TSIPV4ENA: Enable TimeStamp Snapshot for IPv4 frames	12	0x0	When the bit is 1, the time stamp snapshot of IPv6 frame is enabled.
TSIPENA:Enable TimeStamp Snapshot for PTP overEthernet frames	11	0x0	When the bit is 1, the PTP packet (PTP over Ethernet) in the format of Ethernet enables Time Stamp Snapshot; when the bit is 0, the PTP packet in the format of UDP-IP-Ethernet enables Time Stamp Snapshot.
TSCTRLSSR: Time Stamp Digital or Binary rollover control	9	0x0	When the bit is 1, Time Stamp Low register updates and adds the time stamp after its value exceeds 0x3B9A_C9FF; when the bit is 0, the Time Stamp Low register is reset to 0x7FFF_FFFF.
TSENALL: Enable Time Stamp for All Frames	8	0x0	When the bit is 1, it indicates that all frames received by MACs enable the time stamp.
Reserved	7:6	0x0	Reserved
TSADDREG: Addend Reg Update	5	0x0	When the bit is 1, the value of Time Stamp Addend register is used to update PTP block for fine correction. When the updating finishes, this bit is 0.
TSTRIG: Time Stamp Interrupt Trigger Enable	4	0x0	When the bit is 1, if the system time is larger than the value of Target Time register, one time stamp interrupt is generated; after the generation of interrupt, this bit is reset to 0.
TSUPDT: Time Stamp Update	3	0x0	When the bit is 1, based on the values of Time Stamp High Update and Time Stamp Low Update registers, the system updates the current system time, and after this the bit is 0.
TSINIT: Time Stamp Initialize	2	0x0	When the bit is 1, based on the values of Time Stamp High Update and Time Stamp Low Update registers, the system initializes the current system time, and after this the bit is 0.
TSCFUPDT: Time Stamp Fineor Coarse Update Time Stamp Fineor Coarse updating	1	0x0	When the bit is 1, it indicates that the Time Stamp will adopt the Fine Update, and when the bit is 0, it indicates that the Time Stamp will use Coarse.
TSENA: Time Stamp Enable	1	0x0	When the bit is 1, it indicates the receive and transmit frame systems will enable the Time Stamp record; when the bit is 0, it indicates the Time Stamp record is stopped for receive and transmit frames, and the Time Stamp generator is paused; after the bit is set to 1, the Time Stamp Initialization starts (bit 2).

11.2.23 Register449 (Sub-Second Increment Register)

Register449 (Sub-Second Increment Register)Offset: 0x0704			
Reserved	31:8	0x0	Reserved
SSINC: Sub-second increment value	7:0	0x0	The value in this domain will be added to sub-second register

11.2.24 Register 450 (System Time - Seconds Register)

Register 450 (System Time - Seconds Register)Offset: 0x0708			
TTSS: Time Stamp Second	31:0	0x0	The value of this domain indicates the second count of the current system time

11.2.25 Register 451 (System Time - Nanoseconds Register)

Register 451 (System Time - Nanoseconds Register) Offset: 0x0C			
PSNT: Positive or Negative Time	31	0x0	This domain indicates the positive or negative time. When the bit is 1, it indicates the time is positive. When the bit is 0, it indicates the time is negative.
TSSS: Time Stamp Sub Seconds	30:0	0x0	The value of this domain indicates the sub-second count of the current system time, and time precision is 0.46 nanosecond by default (when the TSCTRLSSR asserts the start precision to 1ns, the maximum is 0x3B9A_C9FF)

11.2.26 Register 452 (System Time - Seconds Update Register)

Register 452 (System Time - Seconds Update Register)Offset: 0x0710			
TTSS: Time Stamp Second	31:0	0x0	The value of this domain is the initial value of system initialization or the increment in updating

11.2.27 Register 453 (System Time - Nanoseconds Update Register)

Register 453 (System Time - Nanoseconds Update Register)Offset: 0x0714			
ADDSUB:Add or subtract time	31	0x0	This domain indicates adding or subtracting time. When the bit is 1, it indicates the updated register value is subtracted in updating. When the bit is 0, it indicates the updated register value is added.
TSSS: Time Stamp Sub Seconds	30:0	0x0	The value of this domain indicates the sub-second count is added or reduced when the current system time updates, and the time precision is 0.46 nanosecond by default (when the TSCTRLSSR sets the start precision to 1ns, the maximum is 0x3B9A_C9FF)

11.2.28 Register 454 (Time Stamp Addend Register)

Register 454 (Time Stamp Addend Register)Offset: 0x0718			
TAR: Time Stamp Addend Register	31:0	0x0	The value of this domain indicates that the 32bit time value to add in system time synchronization

11.2.29 Register 455 (Target Time Seconds Register)

Register 455 (Target Time Seconds Register)Offset: 0x1C			
TSTR: Target Time Seconds Register	31:0	0x0	This domain has saved the time in the unit of second. When the time stamp time matches or exceeds the value of this field and low bit register (reg 456) and includes MAC address matching, the system will generate an interrupt (the interrupt must be enabled in advance)

11.2.30 Register 456 (Target Time Nanoseconds Register)

Register 456 (Target Time Nanoseconds Register)Offset: 0x02			
Reserve	31	0x0	
TSTR: Target Time Stamp Low Register	30:0	0x0	This domain has saved the time in the unit of second. When the time stamp time matches or exceeds the value of this field and low bit register (reg 455) and includes MAC address matching, the system will generate an interrupt (the interrupt must be enabled in advance)

11.2.31 Register 457 (System Time - Higher Word Seconds Register)

Register 457 (System Time - Higher Word Seconds Register)Offset: 0x24			
Reserve	31:16	0x0	
TSHWR:Time Stamp Higher Word Register	15:0	0x0	This domain saves the time stamp of high 16bit (most significant bit)

11.2.32 Register 458 (Time Stamp Status Register)

Register 458 (Time Stamp Status Register)Offset: 0x02			
Reserve	31:28	0x0	
ATSNS:Auxiliary Time Stamp Number of Snapshots	27:25	0x0	This domain indicates the number of snapshots in FIFO, 4(3`b100) FIFO full, and 0(3`000) FIFO empty
ATSSTM: Auxiliary Time Stamp Snapshot Trigger Missed	24	0x0	When the bit is 1, it indicates the current FIFO is full and has set the external trigger, and the last snapshot is missed because of FIFO full; or, it's 0.
Reserve	23:3	0x0	
AuxiliaryTime StampTrigger Snapshot	2	0x0	When the bit is 1, it indicates the snapshot is written to FIFO.
TSTARGT:Time Stamp Target Time Reached	1	0x0	When the bit is 1, the system time has exceeded or is equal to the value of target time stamp register
TSSOVF:Time StampSeconds Overflow	0	0x0	When the bit is 1, it indicates the time of the current time stamp has overflowed (larger than 0xFFFF_FFFF); or, it's 0.

11.2.33 Register 459 (PPS Control Register)

Register 459 (PPS Control Register)Offset: 0x0C			
Reserve	31:4	0x0	
PPSCTRL: Control the duration between 2-pulses of PPS signa output	15:0	0x0	This domain sets the time interval of two PPS signals output, and is encoded as follows 0000: 1.0s (Binary & Digital Rollover) 0001: 0.5s (Binary Rollover) , 0.536s (Digital Rollover) 0010: 0.25 s (Binary Rollover) , 0.26s (Digital Rollover) 0011: 0.125 s (Binary Rollover) , 0.26s (Digital Rollover) …..

			1111: 15.28μs (Binary Rollover), 32.77μs (Digital Rollover)

11.2.34 Register 460 (PPS Auxiliary Time Stamp - Nanoseconds Register)

Register 460 (PPS Auxiliary Time Stamp - Nanoseconds Register)Offset: 0x0730			
	31:0	0x0	Includes the low (nanosecond)32bit of Auxiliary Time Stamp

11.2.35 Register 461 (PPS Auxiliary Time Stamp - Seconds Register)

Register 460 (PPS Auxiliary Time Stamp - Seconds Register)Offset: 0x0730			
	31:0	0x0	Include the low (nanosecond)32-bit of Auxiliary Time Stamp

11.3 DMA Descriptor

DMA descriptor is the interactive interface of MAC drive and hardware, and records the memory address and transfer status of data packet. Two data structures: Tx Descriptor and Rx Descriptor have been defined respectively. Two descriptors can freely select the connection in ring mode or chain mode for MAC.

11.3.1 Basic Format of DMA Descriptor

Each DMA descriptor includes two data buffers, two byte count buffer, and two pointer of data buffer address. Note: the descriptor address must guarantee that the connected system bus bit width is aligned and the system byte order is the same (little end by default)

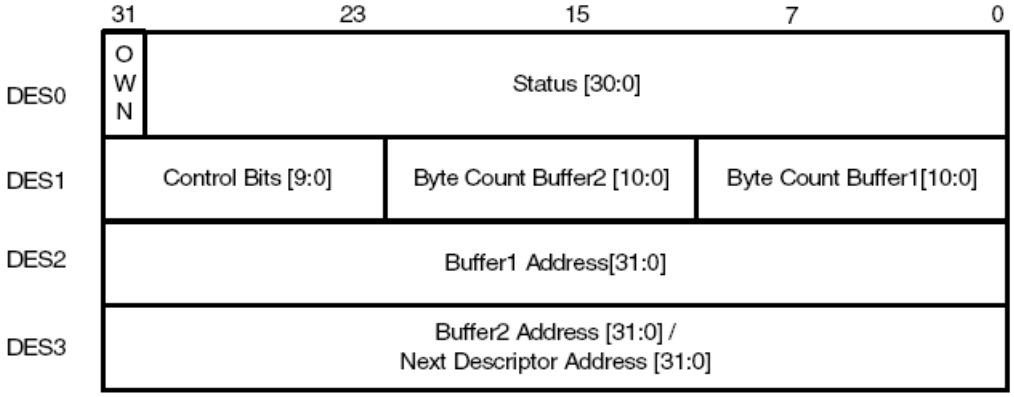

Figure 11-1 Basic format of DMA descriptor (little end 32bit bus)

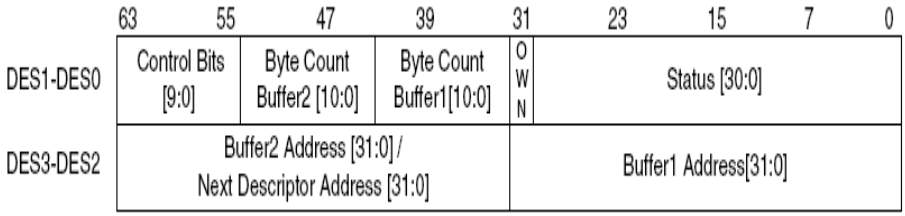

Figure 11-2 Basic format of DMA descriptor (little end 32bit bus)

11.3.2 DMA receive descriptor

CMAC subsystem needs at least two receive descriptors in operating mode to normally receive one network data packet. When processing one network data packet, its internal receive module always tries to obtain the next receive descriptor. Each network data packet is called one frame.

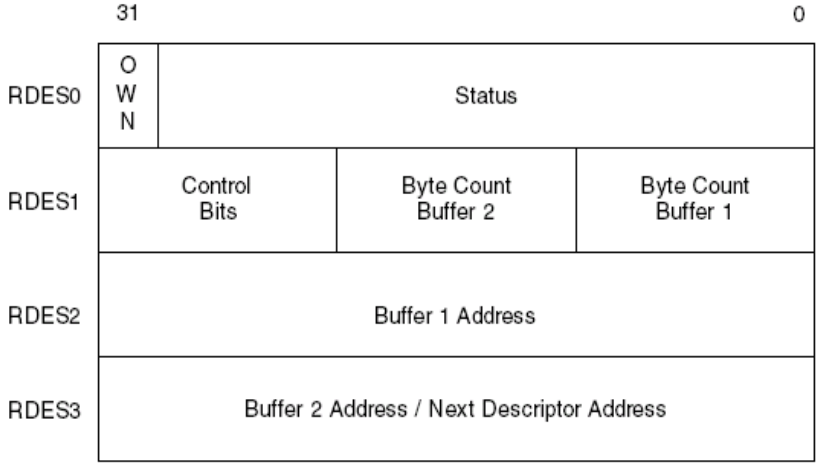

Figure 11-3 Basic format of DMA receive descriptor (small end 32bit bus)

11.3.2.1 RDES0

RDES0 includes the current receive frame status, length and all circumstances of the descriptor (owned by host or DMA). Details of RDES0 see table below.

RDES0 bit		
OWN All modes	31	When the bit is 1, it indicates the descriptor belongs to DMA control, and when the bit is 0, it indicates the descriptor belongs to DMA control. When DMA module finishes one transmission, the bit will be cleared automatically.
AFM: Destination Address Filter 1	30	When the bit is 1, it indicates that the current data frame target address doesn't comply with the internal frame target address filter of GMAC.
FR: Frame length Frame length	29:16	It indicates receiving the length of the current frame. When ES bit is 0, it's significant.
ES: Error Summary	15	It indicates whether the current frame is wrong, and its value is RDES[0], RDES[1], RDES[3], RDES[4], RDES[6], RDES[7], RDES[11] and RDES[14] bits or (OR) operation.
DE: Descriptor Error	14	When the bit is 1, it indicates that the buffer pointed by current descriptor doesn't comply with the frame or OWN is 0 (host control)
SAF: Source Address Filter Fail	13	When the bit is 1, it indicates that the current data frame target address doesn't comply with the internal frame source address filter of GMAC.
LE: Length Error	12	When the bit is 1, it indicates that the length of the current receive frame doesn't comply with the default length. When the Frame Type bit is 1, and CRC Error bit is 0, it's significant.
OE: Over Flow Error	11	When the bit is 1, it indicates that when the frame is received, GMAC internal RxFIFO overflow.
VLAN: VLAN Tag	10	When the bit is 1, it indicates the frame type is VLAN.
FS: First Desciptor	9	When the bit is 1, it indicates the buffer pointed by current descriptor is the first saved buffer of the current receive frame.
LS: Last Descriptor	8	When the bit is 1, it indicates the buffer pointed by current

		descriptor is the last saved buffer of the current receive frame.
IPC Checksum Error/Giant Frame	7	When the bit is 1, if IPC check function is enabled, it indicates that the IPv4 head check value of the current frame doesn't comply with the value of frame internal check domain. If it's disabled, it indicates that the current frame is a giant frame (more than 1518 bytes long)
LC: Late collision	6	When the bit is 1, it indicates that in half-duplex mode, when the current frame receives, one late collision occurs.
FT: Frame Type	5	When the bit is 1, it indicates the current frame is an Ethernet frame. When the bit is 0, it indicates the current frame is a IEEE802.3 frame.
RIWT: Receive Watchdog Timeout	4	When the bit is 1, it indicates the current clock value exceeds the value of Watchdog circuit clock in receive module, namely, the receive frame timeout
RE: Receive Error	3	When the bit is 1, it indicates the internal module goes wrong when receiving the current frame. Internal signal Rxer is set to 1 and rxdv is set to 1
DE: Dribble bit Error	2	When the bit is 2, it indicates the length of the receive frame isn't an integer, namely, the total length is an odd bit. It's significant only in mii mode.
CE: CRC Error	1	When the bit is 1, it indicates the internal CRC goes wrong when receiving the current frame. Only in last descriptor(RDES0[8], this bit is significant.
RX MAC: Checksum/payload Checksum Error	0	When the bit is 1, it indicates when receiving the current frame, the internal RX MAC register block 1-15 has one address matching the current frame. When the bit is 0, it indicates the RX MAC register block 0 matches the receive frame destination address. When Full Checksum Offload Engine is enabled, if the bit is 1, it indicates the frame TCP/UDP/ICMP check error. When the bit is 1, it also indicates the current frame actual receive length doesn't comply with the internal record length.

11.3.2.2RDES1

RDES1 has recorded the buffer size pointed by descriptor, and the organization form of the descriptor (ring or chain).

RDES1 bit		
Disable Intr in Completion	31	When the bit is 1, it indicates after the frame receive completes, the RI bit (CSR5[6]) in STATUS register won't be set. In this way, the host can't detect such interrupt.
Reserved	30:26	
RER: Receive End of Ring	25	When the bit is 1, it indicates the descriptor is the last in the ring descriptor link table, and the address of the next descriptor is the base address of the receive descriptor.
RCH: Second Address Chained The second buffer also points to the next chain descriptor	24	When the bit is 1, it indicates that the second buffer address in descriptor points the address of the next descriptor. When the bit is 0, it indicates the address points to the second buffer address. When the bit is 1, the value of RDES1[21-11] is insignificant, and RDES1[25] has a higher priority than RDES1[24](represent ring instead of chain)
Reserved	23:22	
RBS2: Receive Buffer Size 2	21:11	This domain indicates the size of data buffer2. Based on the width 32/64/128 of the system bus, the size of buffer2 should be integral multiples of 4/8/16. Unknown results will be caused if there is no satisfaction. When the domain in RDES1[24] is 0, it's significant.

RBS2: Receive Buffer Size 1	10:0	This domain indicates the size of data buffer1. Based on the width 32/64/128 of the system bus, the size of buffer1 should be integral multiples of 4/8/16. Unknown results will be caused if there is no satisfaction. This domain has always been valid. If the threshold is 0, DMA will automatically access buffer 1 or the next receive descriptor.

11.3.2.3RDES2

This domain has recorded the address of data receive buffer 1.

RDES2 bit		
Buffer1 Address Pointer	31:0	The field has recorded the 32bit physical address of data receive buffer1. The physical address has no default alignment requirements. When CMAC DMA aligns the bus data 32/64/128 bit, the low 2/3/4 bit of the address is ignored.

11.3.2.4 RDES3

This domain has recorded the address of data receive buffer 2.

RDES3 bit		
Buffer2 Address Pointer	31:0	The field has recorded the 32-bit physical address of data receive buffer2. The physical address has no default alignment requirements. When CMAC DMA aligns the bus data 32/64/128 bit. If the descriptor in connected by chain, the field records the address of the next descriptor.

11.3.3 DMA transmit descriptor

The formats of transit descriptor and receive descriptor are basically same. Each descriptor address need to be aligned based on bus width (32/64/126bits).

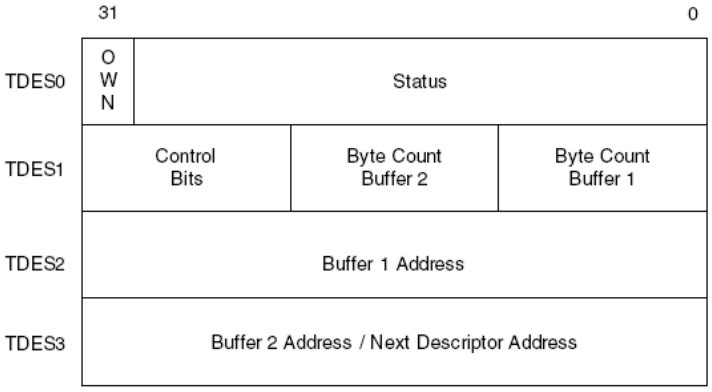

Figure 11-4 Basic format of DMA transmit descriptor (little tailing end 32-bit bus)

11.3.3.1TDES0

TDES0 includes the state of transmit frame and messages of transmit descriptor.

TDES0 bit		
OWN	31	When the bit is 1, it indicates the descriptor belongs to DMA control, and when the bit is 0, it indicates the descriptor belongs

		to DMA control. When DMA module finishes one transmission, the bit will be cleared automatically.
Reserved	30:18	
TTSS: Tx Time Stamp Status	17	When IEEE1588 function is enabled, if the bit is 1, it indicates the time stamp message of this transmit frame has been saved in TDES2 and TDES3. Or the bit shall be reserved
IHE: IP Header	16	When the bit is 1, it indicates the internal check module finds the wrong IP head of this transmit frame, and won't change the domain.
ES: Error Summary	15	It indicates whether the current frame is wrong, and its value is RDES[0], RDES[1], RDES[3], RDES[4], RDES[6], RDES[7], RDES[11] and RDES[14] bits or (OR) operation.
JT: Jabber Timeout	14	When the bit is 1, it indicates GMAC transmit module encounters Jabber timeout.
FF Frame Flushed	13	When the bit is 1, it indicates the software sends a refresh command, and cause DMA/MTL to refresh all internal frames.
PCE: Payload	12	When the bit is 1, it indicates the internal loading check mode insert the check number in the transmit frame
Checksum Error		It is an error. This bit is significant when the load check module is enabled
LC: Loss of Carrier	11	When the bit is 1, it indicates the carried signal is lost during frame transmission (gmii_crs signal several cycles aren't set)
NC: No Carrier	10	When the bit is 1, it indicates that the carried signal of PHY has been set during transmission.
LC: Late Collision	9	When the bit is 1, it indicates that in half-duplex mode, when the current frame receives, one late collision occurs.
EC: Excessive Collision	8	When the frame is 1, it indicates 16 collisions occur before the current frame is sent.
VF: VLAN Frame VLAN frames	7	When the bit is 1, it indicates that the current transmit frame is a VLAN frame.
CC Collsion Count	6:3	This domain indicates the total collision number before the successful transmission of the current frame
ED: Excessive Deferral	2	When this bit is 1, it indicates current frame transmission is completed.
UF: Underflow Error	1	When the bit is 1, it indicates that overflow error occurs in current frame transmission, namely, data transmission. buffer is too small or unavailable
DB: Defered Bit Frame Flushed	0	When the bit is 1, it indicates that the transmission is delayed, and it's only significant in half-duplex mode.

11.3.3.2TDES1

TSESI includes the buffer size and other control and status bits of some descriptor ring/chain connection.

TDES1 bit		
IC: Interruption on Complete	31	When the bit is 1, it indicates that after the frame transmit finishes, the TI bit in STATUS register will be set (CSR5[0])
LS: Last Segment	30	When the bit is 1, it indicates the current buffer includes the last segment of one frame data (if the frame is divided into several segments)
FS: First Segment	29	When the bit is 1, it indicates the current buffer includes the first segment of one frame data (if the frame is divided into several segments)
CIC: Checksum Insertion Control	28:27	This domain controls whether the control internal module fills out check data in transmit frame. Value: 2'b00: No insertion checksum

		2'b01: Insertion IPV4 header checksum 2'b10: When the pseudo-header exists, TCP/UDP/ICMP full check data are filled out. 2'b11: TCP/UDP/ICMP full check data are always filled out.
DC Disable CRC	26	When the bit is 1, CMAC hardware doesn't add CRC check data at the end of each transmit frame.
TER: Transmit End of Ring Descriptor	25	When the bit is 1, it indicates the descriptor is the last in the ring descriptor link table, and the address of the next descriptor is the base address of the transmission descriptor.
TCH: Second Address Chained The second buffer address pointer	24	When the bit is 1, it indicates that the second buffer address in descriptor points the address of the next descriptor. When the bit is 0, it indicates the address points to the second buffer address. When the bit is 1, the value of RDES1[21-11] is insignificant, and RDES1[25] has a higher priority than RDES1[24](represent ring instead of chain)
DP: Disable Padding	23	When the bit is 1, it indicates the GMAC won't fill out the empty data in data packet with the length smaller than 64 bytes
TTSE: Transmit Time Stamp Enable	22	When the bit is 1, the internal module will be started to compute IEEE1588 hardware time stamp, and when TDES1[29] is 1, it's significant.
TBS2: Transmit Buffer Size 2	21:11	This domain indicates the size of data buffer2. When TDES1[24] is 1, this domain is insignificant.
TBS1: Transmit Buffer Size 1	10:0	This domain indicates the size of data buffer1. This domain has always been valid. If the threshold is 0, DMA will automatically access buffer 1 or the next receive descriptor.

11.3.3.3TDES2

This domain has recorded the address of data transmission buffer 1.

TDES2 bit		
Buffer1 Address Pointer Transmit buffer1 address	31:0	The field has recorded the 32bit physical address of data receive buffer1. The physical address has no default alignment requirements. When CMAC DMA aligns the bus data 32/64/128 bit, the low 2/3/4 bit of the address is ignored.

11.3.3.4TDES3

This domain has recorded the address of data transmission buffer 2.

TDES3 bit		
Buffer2 Address Pointer Transmit buffer2 address	31:0	The field has recorded the 32-bit physical address of data receive buffer2. The physical address has no default alignment requirements. When CMAC DMA aligns the bus data 32/64/128 bit, the low 2/3/4-bit of the address is ignored. If the descriptor is connected by chain, this domain records the address of the next descriptor.

11.4 Software Programming Guide

DMA initialization:

1 Software reset (reset) MAC
2. Wait for reset completion (search DMA reg0[0])
3. Program the following domain of DMA reg0
a. MIX-BURST and AAL(DMA reg0[26], [25])
b. Fixed-burst or undefined-burst(DMA reg0[16])
c. Burst-length and Burst-mode

d. Descriptor Length (Only in ring, is it effective)
e. Tx and Rx arbitration scheduling
4. Program AXI Bus Mode Reg
a. If the Fixed-burst is selected, it's necessary to set the maximum burst length in the register.
5. It has created the transmit and receive descriptor chains respectively, and chosen ring mode or chain mode for connection, and their OWN bits of receive descriptor is set to 1 (owned by DMA)
6. Before the software enables DMA descriptor, it must guarantee three are at least three descriptors in transmit/send descriptor.
7. Write the starting address of the receive and transmit descriptor chain tables to DMA reg 3, 4
8. Configure the following bit in DMA reg6(DMA mode operation)
a. Received/transmitted Store and Forward
b. Received/transmitted threshold control
c. Hardware flow control enable
d. Error frame and unidentified correct frame skipping (forwarding enable)
e. OSF mode
9. Write 1 to DMA reg6(Status reg), and clear all interrupt requests
10. Write 1 to DMA reg7(interrupt enable reg), and enable all interrupts
11. Write 1 to DMA reg6[1], [13], enable transmit and receive DMA

MAC initialization:
1 Correctly configure the supporting PHY chips
2. Correctly configure MAC reg4(GMII Address Register), make it normally access PHY related register
3. Read MAC reg5(GMII Data Register) to obtain messages such as link, speed and mode (duplex) of the current PHY
4 Configure MAC address
5. If the harsh filtering is enabled, it's necessary to configure the hash filtering
6. Configure the following domain of MAC reg1(Mac Frame filter), conduct the frame filtering
a. Receive all
b. Promiscuous mode
c. Hash or perfect filter
d. Groupcast and multicast filter settings, etc.
7. Configure the following domain of MAC reg6(Flow control register)
a. Pause time and other pause control bit
b. Receive and transmit flow control bit
C. Busy flow control / follow-up pressure enable
8. Configure the interrupt mask register (Mac reg15)
9. Rightly configure MAC reg0 based on previously obtained line message (link, speed, mode)
10. Configure MAC reg0[2], [3] to enable transmit and enable modules in MAC

General processes of transmit and receive:
1. After detecting transmit or receive interrupt, search the corresponding descriptor to judge whether it belongs to host, and read the data in descriptor
2. After finishing reading the data in descriptor, clear all descriptor bits and set their OWN bits, and make it continue transmitting/receiving data
3. If the current transmit or receive descriptors don't belong to DMA(OWN=0), the DMA module will enter into the suspended state. When the data need transmitting/receiving, write 1 to DMA Tx/Rx POLL register, and enable DMA module again Note: the receive descriptor should always belong to DMA(OWN=1) when idle.
4. Transmit and receive descriptors comply with the real-time information of corresponding buffer address, and can be obtained by searching DMA reg18, 19, 20, 21.

11.5 IEEE 1588 Support

MAC controller supports IEEE 1588 clock synchronous protocol. IEEE 1588 defines that the protocol with technologies such as LAN, distributed object to implement accurate clock synchronous proofreading, measuring and control systems. IEEE1588 protocol is widely applicable to support heterogeneous systems with different

clock characteristics, and provide the full-system sub-second precision synchronization. The following two figures provide two different clock system synchronization based on IEEE1588 protocol. Figure 1 is the process where the host cycle sends the synchronous message to all slave devices in internet, and Figure 2 is the process that the slave synchronizes the host synchronously.

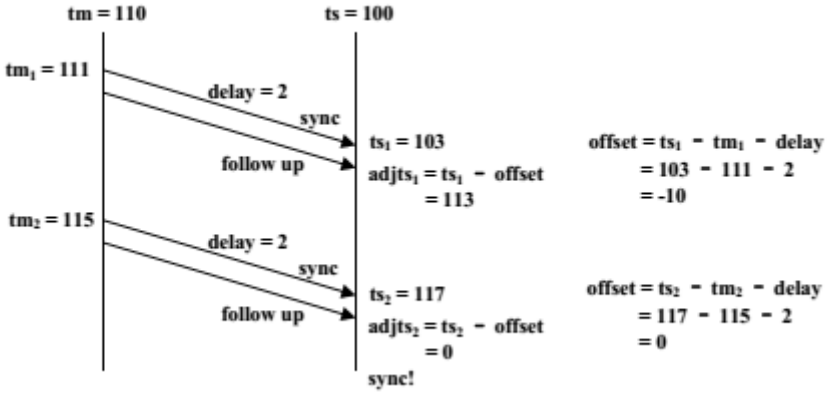

Figure 11-5 Period clock synchronization process

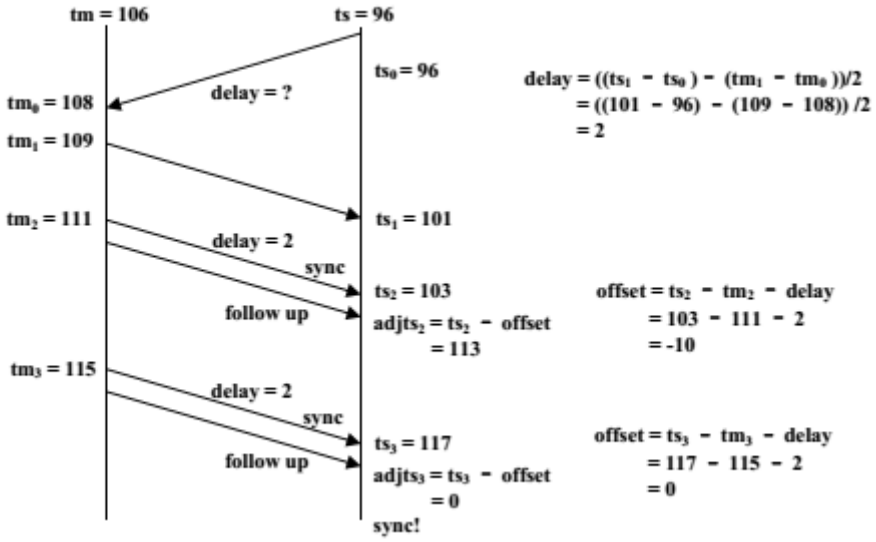

Figure 11-6 Slave proactive synchronization process

During the synchronization of master and slave devices, the sent message frame is called ptp (precious time protocol). See IEEE1588 protocol for the specific synchronization process. The entire clock synchronization proofreading process is basically finished in internet UDP protocol layer, and MAC controller hardware only needs to support the transmit and receive time functions of ptp packets, namely, the tm/s in above figure.

IEEE1588 software programming guide:

To enable IEEE1588 time stamp function, set Register 448 Time Stamp Control Register bit0 to 1. But in order to use the function normally, the following relevant initialization work must be completed in MAC initialization phase:

IEEE1588 initialization:
1. Set the bit9 of register 15 to 1, and switch off the system interrupt triggered by time stamp.
2. Set the bit0 of time stamp control register (reg 448) to 1, and enable time stamp function.
3. Set Register 449 Sub-Second Increment Register based on ptp clock frequency.
4. If you use Fine Correction approach, set register (Register 454 Time Stamp Addend register) and set the bit 5 of

time stamp control register (reg 448) to 1 (addend reg update)
5. The bit5 of rolling time stamp control register is set to 0.
6. Enable the Fine Update method by setting the bit1 of time stamp control register to 1 (if necessary).
7. Set the Time Stamp High Update and Time Stamp Low Update to corresponding values.
8. Set the bit2 of time stamp control register to 1 (time stamp initialization)
9. When writing the initial value to time stamp update register (registers 452 and 453 Time Stamp Update register), the time stamp counter starts to work.
10. Enable transmit and receive modules of MAC to correctly operate time stamp function.
Note: when IEEE1588 function is disabled, follow and execute the above process to restart it.

System clock correction:
To synchronize or update the system clock in a process (coarse correction method), the following procedures are adopted:
1. Write the offset (positive or negative) to time stamp update register (registers 452 and 453 Time Stamp Update registers)
2. Set the bit3 of time stamp control register (reg 448) to 1.
3. When the bit of TSUPDT (reg448bit3) becomes 0, system clock adds or subtracts the offset in time stamp update register in procedure 1.

12 USB Controller

12.1 Overview

Characteristics of USB host port 1C is as follows:

- It's **compatible** with USB Rev 1.1 and USB Rev 2.0 protocols
- It's **compatible** with OHCI Rev 1.0 and EHCI Rev 1.0 protocols
- Support the USB device at LS (Low Speed) , FS (Full Speed) and HS (HighSpeed)
- Support one port, and suspend LS, FS or HS device.

USB host controller module includes a EHCI controller supporting HS device, and one OHCI controller supports FS and LS devices. Therein, the EHCI controller is in master control status, and only when FS or LS devices are suspended, can the control right be transferred to OHCI controller; only when FS or LS device is pulled up, will control right return to EHCI controller.

Meanwhile, the USB controller has integrated the AHB bus interface (compatible with AMBA Specification Revision 2.0) for the communication with memory/application. The interconnection architecture chart of USB controller and the outside is as shown in Figure 12-1:

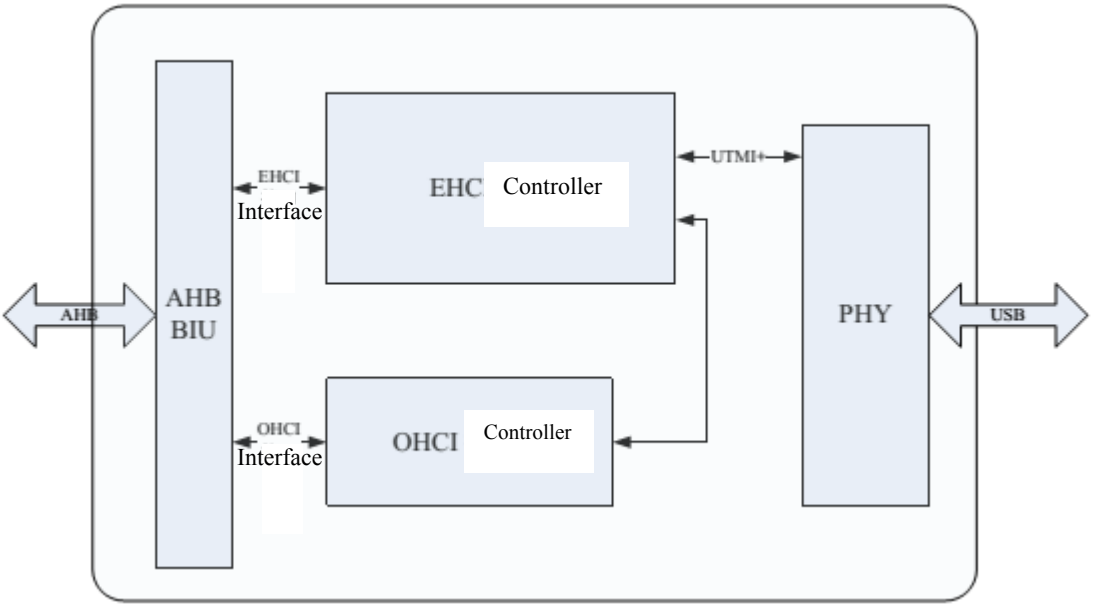

Figure 12-1 USB host controller module

12.2 USB Host Controller Register

12.2.1 EHCI relevant registers

EHCI relevant registers include Capacity register, Operational register and EHCI implementation relevant register. The USB host controller of 1C is compatible with EHCI Rev 1.0 protocol. For Capacity register and Operational register, please refer to Enhanced Host Controller Interface Rev 1.0 Specification.

The base address of EHCI is equal to the base address of the below register plus offset.

12.2.2 Capability register

Name	Offset address	Width	Access	Note
HCCAPBASE	0x00	32	RO	The value is 32'h01000010 by default.

HCSPARAMS	0x04	32	RO	The value is 32'h00001116 by default.
HCCPARAMS	0x08	32	RO	The value is 32'h0000A010 by default.

(Notes: USBBase is fixed as the starting address 0xbfe2_0000 of EHCI slave)

12.2.3 Operational Register

Name	Address	Width	Access	Note
USBCMD	0x10	32	R/W RO	USB host controller command register
USBSTS	0x14	32	R/W RO	USB host controller status register
USBINTR	0x18	32	R/W	Interrupt set register of USB host controller
FRINDEX	0x1C	32	R/W	USB host controller frame index register
CTRLDSSEGMENT	0x02	32	R/W	Store the address of EHCI control data structure
PERIODICLISTBASE	0x24	32	R/W	Store the initial address of period data frame table
ASYNCLISTADDR	0x28	32	R/W	Store the initial address of the next asynchronous queue to execute
CONFIGFLAG	0x05	32	R/W	Configuration mode register
PORTSC 1	0x54	32	R/W	Port 1 status and control register
PORTSC 2	0x58	32	R/W	Port 2 status and control register
PORTSC 3	0x5c	32	R/W	Port 3 status and control register
PORTSC 4	0x60	32	R/W	Port 4 status and control register
PORTSC 5	0x64	32	R/W	Port 5 status and control register
PORTSC 6	0x88	32	R/W	Port 6 status and control register

(Notes: USBOPBase is fixed as the starting address of EHCI slave + `h10)

12.2.4 EHCI implementation relevant register

EHCI implementation relevant register is described as follows.

Name	Address	Width	Access	Note
INSNREG00	0x90	32	R/W	**Frame length configuration register**
INSNREG01	0x94	32	R/W	**Data packet buffer OUT/IN threshold register**
INSNREG02	0x98	32	RO	**Data packet buffer depth register**
INSNREG03	0x9c	32	R/W	Reference to the detailed register description
INSNREG04	0xa0	32	R/W	For Debug
INSNREG05	0xa4	32	R/W	UTMI configuration (default setting) , control and status registers
INSNREG06	0xa8	32	RO	AHB error status register
INSNREG07	0xa:	32	RO	AHB Master error address register

INSNREG08	0xb0	32	RO	HSIC enable register

INSNREG00 register (disable)

INSNREG01 register

Bit field	Access	Reset value	Note
31:16	R/W	16'h0020	OUT threshold (the unit is 4 bytes). Once the data fetched from system memory reaches the OUT threshold, the USB transmission starts, at least 16bytes.
15:0	R/W	16'h0020	IN threshold (the unit is 4 bytes). Once the data fetched from Packet Buffer reaches the IN threshold, the USB transmission starts, at least 16bytes.

INSNREG02 register

Bit field	Access	Reset value	Note
31:12	Reserved	20'h0	Reserved
11:0	RO	12'h0020	**Data packet buffer depth** (the unit is 4 bytes)

INSNREG03 register

Bit field	Access	Reset value	Note
31:13	Reserved	19'h0	Reserved
12:10	RO	3'h0	When the field defines the extra delay of phy_clks, the delay is added to “Tx-Tx turnaround Delay”.
9	RO	1'h0	Set 1: to force the host controller to obtain the cycle data frame table for each micro-frame in a frame Set 0: the host controller obtains the cycle data frame table from each micro-frame 0 in a frame
8:1	R/W	8'h0	The time can tolerate the offset, and the field is used to indicate the byte number to add for tolerating and computing the available time. To computer the available time is added for the future transmission elasticity, and the user program default doesn’t need to change this field.
0	RO	1'h0	Break Memory Transaction mode Set to 1: enable this function Set to 0: disable this function

INSNRE04 register (it’s only used for debugging, and the software doesn’t need to change this register)

Bit field	Access	Reset value	Note
31:6	Reserved	26'h0	Reserved
5	R/W	1'h0	**Set 1: disable automatic function. Namely, when the software clears Run/Stop bit, USB host controller wake up the Suspend port** **Set 0: enable automatic function. When the software rests Run/Stop bit, Suspend signal will be set to 1.**
4	R/W	1'h0	**Set 1: disable NAK reload repair** **Set 0: enable NAK reload repair**
3	Reserved	1'h0	Reserved
2	R/W	1'h0	Set 1: shorten port enumeration time (simulation)
1	R/W	1'h0	Set to 1: 17, 15:4 and 2:0 bits in HCCPARAMS register can be written
0	R/W	1'h0	Set to 1: HCSPARAMS writable register

INSNREG05 register

Bit field	Access	Reset value	Note
31:18	Reserved	14'h0	**Reserved**
17	RO	1'h0	**Set 1: it indicates a write operation is conducted for the register, and the hardware is executing.** **Set to 0: it indicates the hardware has completed the operations**
16:13	R/W	5'h0	**Port number**
12	R/W	4'h1	VControlLoadM Set to 1: NOP Set to 0: Load
11:8	R/W	4'h0	VControl
7:0	RO	4'h0	VStatus

INSNREG06 register

Bit field	Access	Reset value	Note
31	R/W	1'h0	Once AHB make mistakes and is captured, set it 1, write 0 and clear this field.
30:12	Reserved	19'h0	Reserved
11:9	RO	3'h0	In the event of AHB error, the value of HBURST in control field
8:4	RO	5'h0	The burst expected beats of AHB error
3:0	RO	4'h0	In the current burst, the completed beats before AHB error

INSNREG07 register

Bit field	Access	Reset value	Note
31:0	RO	32'h0	AHB control segment address in error

INSNREG08 register

Bit field	Access	Reset value	Note
31:0	RO	1'b0	HSIC enable

12.3 OHCI Relevant Register

OHCI relevant registers include Operational register and OHCI implementation relevant register. The USB host controller of 1C is compatible with OHCI Rev 1.0 protocol. For Operational register details, please refer to Open Host Controller Interface Rev 1.0 Specification.

The base address of OHCI is 0xbfe280000 and the address of the below register is equal to the base address plus offset.

12.3.1 Operational Register

Name	**Address**	**Width**	**Access**	**Note**
HcRevision	0x00	32	-	Control and status
HcControl	0x04	32	-	
HcCommonStatus	0x08	32	-	
HcInterruptStatus	0x0C	32	-	
HcInterruptEnable	0x10	32	-	
HcInterruptDisable	0x14	32	--	

HcHCCA	0x18	32	-	Memory pointer
HcPeriodCuttentED	0x1C	32	-	
HcControlHeadED	0x20	32	–	
HcControlCurrentED	0x24	32	–	
HcBulkHeadED	0x28	32	–	
HcBulkCurrentED	0x2C	32	–	
HcDoneHead	0x30	32	–	
HcRmInterval	0x34	32	–	Frame counter
HcFmRemaining	0x38	32	–	
HcFmNumber	0x3C	32	–	
HcPeriodicStart	0x40	32	–	
HcLSThreshold	0x44	32	–	
HcRhDescriptorA	0x48	32	–	Concentrator
HcRhDescriptorB	0x0C	32	–	
HcRhStatus	0x50	32	–	
HcRhPortStatus1	0x54	32	–	
HcRhPortStatus2	0x58	32	–	

12.3.2 OHCI implementation relevant register

Except the standard OHCI operation register, it has also implemented two additional registers (register offset 0x98 and 0x9C) to report the error state of AHB.

Name	Address	Width	Access	Note
INSNREG06	0x98	32	RO	AHB error status register
INSNREG07	0x9c	32	RO	AHB Master error address register

INSNREG06 register

Bit field	Access	Reset value	Note
31	R/W	1'h0	Once AHB make mistakes and is captured, set it to 1, write 0 and clear this field.
30:12	RO	19'h0	**Reserved**
11:9	RO	3'h0	**In the event of AHB error**, the value of HBURST in control field
8:4	RO	5'h0	The burst expected beats of AHB error
3:0	RO	4'h0	In the current burst, the completed beats before AHB error

INSNREG07 register

Bit field	Access	Reset value	Note
31:0	RO	32'h0	AHB control segment address in error

13 OTG Controller

13.1 Overview

1C OTG supporting characteristics are as follows:

- Support HNP and SRP protocols;
- Embedded DMA without occupying processor band width for the mobile data between OTG and external storage
- In device mode, HS device (480Mbps);
- In host mode, it only support HS device (480Mbps);
- In device mode, it supports two directional endpoints, with only the defaulted endpoint0 support control transmission;
- In device mode, it supports the transmission in 2 IN directions at most at the same time;
- In host mode, it supports 6 channels, and the software can set each channel direction.
- In host mode, it supports the periodic OUT transmission.

13.2 Register Description

The application reads and writes the control and status registers (CSRs) in OTG controller by AHB slave interface, and these registers are 32bit wide, and the register address is 32bit aligned.

Note: in host mode and device mode, the accessible register block only includes Core Global register block, Power and Clock Gating register block, Data FIFO Access register block and Host Port register block. When the OTG controller is in host or device mode, the register in another mode can't be accessed. In the event of illegal register read and write, the mode mismatch interrupt will occur, and such interrupt will be reflected in Core Interrupt Register.

When the OTG converts from one mode to another, the register in this mode must be reconfigured, because the status of the register after conversion is the same with that in restart.

The address mapping of CSR is fixed. The registers in Host mode and Device mode are located in different address spaces, and all registers all work in AHB clock field. The figure below displays the address mapping relation of CSR.

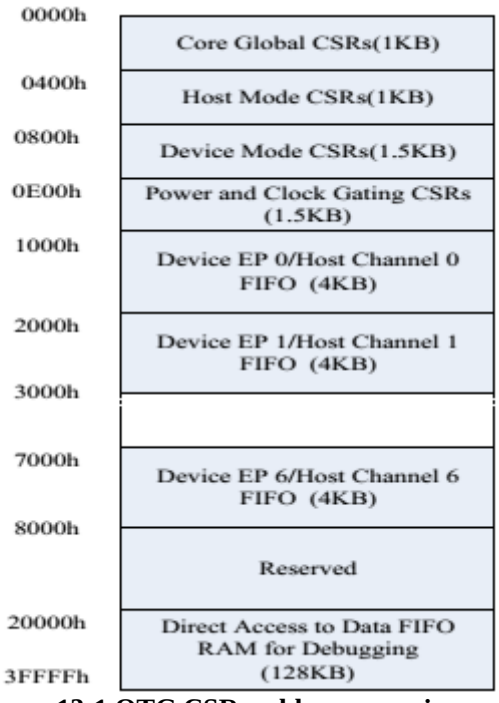

Figure 13-1 OTG CSRs address mapping

The following chapter has listed OTG all registers and their offset address, and their base address is 0xbfe0_0000.

13.2.1 Global Control and Status Registers (Global CSR Map)

No matter whether OTG works in host mode or Device mode, this register block can be accessed, and their corresponding offset addresses are shown in the table below:

Register abbreviated name	Offset address	Register name
GOTGCTL	000h	Control and Status Register
GOTGINT	004h	Interrupt Register
GAHBCFG	008h	AHB Configuration Register
GUSBCFG	00Ch	USB Configuration Register
GRSTCTL	010h	Reset Register
GINTSTS	014h	Interrupt Status Register
GINTMSK	018h	Interrupt Mask Register
GRXSTSR	01Ch	Receive Status Debug Read/Status Read and Pop Registers
GRXSTSP	020h	
GRXFSIZ	024h	Receive FIFO Size Register
GNPTXFSIZ	028h	Non-Periodic Transmit FIFO Size Register
GNPTXSTS	02Ch	Non-Periodic Transmit FIFO/Queue Status Register
GSNPSID	040h	Synopys ID Register
GHWCFG1	044h	User HW Config1 Register
GHWCFG2	048h	User HW Config2 Register
GHWCFG3	04Ch	User HW Config3 Register
GHWCFG4	050h	User HW Config4 Register
GDFIFOCFG	05Ch	DFIFO Software Config Register
HPTXFSIZ	100h	Host Periodic Transmit FIFO Size Register
DIEPTXFn	104h-3FFh	Device IN Endpoint Transmit FIFO Size Register

13.2.2 Host Mode Control and Status Register (Host Mode CSR)

Once OTG operates in Host mode, this register block will be reset.

Register abbreviated name	Offset address	Register name
HCFG	400h	Host Configuration
HFIR	404h	Host Frame Interval Register
HFNUM	408h	Host Frame Number/Frame Time Remaining Register
	40ch	Reserved
HPTXSTS	410h	Host Periodic Transmit FIFO/Queue Status Register
HAINT	414h	Host All Channels Interrupt Register
HAINTMSK	418h	Host All Channels Interrupt Mask Register
HPRT	440h	Host Port Control and Status Register
	444h-4FCh	Reserved
HCCHARn	500h	Moving the Host Core to Test Mode
HCSPLTn	504h	Host Channel-n Split Control Register (HCSPLTn
HCINTn	508h	Host Channel-n Interrupt Register (HCINTn)
HCINTMSKn	50Ch	Host Channel-n Interrupt Mask Register (HCINTMSKn
HCTSIZn	510h	Host Channel-n Transfer Size Register (HCTSIZn

HCDMAn	514h	Host Channel-n DMA Address Register
	518h	Reserved
HCDMABn	51Ch	Host Channel-n DMA Buffer Address Register
HCCHARn	520h–53Ch 540h-55h … 6C0h—6DCh 6E0h-6FCh 6FDh-7FFh	Host Channel-n Characteristics Register

13.2.3 Device Mode Control and Status Register (Device Mode CSR)

Once OTG operates in Device mode, this register block will be reset.

Register abbreviated name	Offset address	Register name
DCFG	800h	Device Configuration Register
DCTL	804h	Device Control Register
DSTS	808h	Device Status Register
	41Ch	Reserved
DIEPMSK	808h	Device IN Endpoint Common Interrupt Mask Register
DOEPMSK	808h	Device OUT Endpoint Common Interrupt Mask Register
DAINT	808h	Device All Endpoints Interrupt Register
DAINTMSK	41Ch	Device All Endpoints Interrupt Mask Register
DVBUSDIS	808h	Device VBUS Discharge Time Register
DVBUSPULSE	41Ch	Device VBUS Pulsing Time Register
DTHRCTL	830h	Device Threshold Control Register
DIEPEPMSK	834h	Device IN Endpoint FIFO Empty Interrupt Mask Register
DIEPCTL0	900h	Device Control IN Endpint0 Control Register
	808h	Reserved
DIEPCTLn	920-AE0h	Device Endpoint-n Control Register
DIEPINTn	808h	Device Endoint-n Interrupt Register
	41Ch	Reserved
DIEPTSIZ0/DOEPTSIZ0	808h	Device Endpoint0 Transfer Size Register
DIEPTSIZn/DOEPTSIZn	808h	Device Endpointn Transfer Size Register
DIEPDMAn	808h	Device Endpoint-n DMA Address Register
DTXFSTSn	808h	Device IN Endpoint Transmit FIFO Status Register
DIEPDMAB0	41Ch	Device Endpoint-n DMA Buffer Address Register
DOEPCTL0	B00h	Device Control OUT Endpint0 Control Register
	B04h	Reserved
DOEPCTLn	B20-BE0h	Device Endpoint-n Control Register
DOEPINTn	B08h	Device Endoint-n Interrupt Register
	B0Ch	Reserved
DOEPTSIZ0	B10h	Device Endpoint0 Transfer Size Register
DOEPTSIZn	B10h	Device Endpointn Transfer Size Register
DOEPDMAn	B14h-CF4h	Device Endpoint-n DMA Address Register
DOEPDMAB0	B1Ch-CFCh	Device Endpoint-n DMA Buffer Address Register

13.2.4 Data FIFO Access Register MAP (DFIFO Access Register MAP)

No matter whether OTG operates in Host mode or Device mode, this register block can be accessed. This register block is used to read and write the FIFO of endpoint or channel in given direction. In host mode, the FIFO in channel direction is IN, and only the FIFO in this channel can be read; similarly, in host mode, the FIFO in

channel direction is OUT, and only the FIFO in this channel can be written.

Register name	Offset address	Read-write characteristics
Device IN Endpoint 0/Host OUT Channel 0: DFIFO Write Access Device OUT Enpoint 0/Host IN Channel 0: DFIFO Read Access	1000h-1FFCh	WO/RO
Device IN Endpoint 0/Host OUT Channel 0: DFIFO Write Access Device OUT Enpoint 0/Host IN Channel 0: DFIFO Read Access	2000h-2FFCh	WO/RO
Device IN Endpoint 14/Host OUT Channel 14: DFIFO Write Access Device OUT Enpoint 14/Host IN Channel 14: DFIFO Read Access	F000h-FFFCh	WO/RO
Device IN Endpoint 15/Host OUT Channel 15: DFIFO Write Access Device OUT Enpoint 15/Host IN Channel 15: DFIFO Read Access	10000h-10FFCh	WO/RO

13.2.5 Power and Clock Gating CSR Map

No matter whether OTG operates in Host mode or Device mode, this register block can be accessed. This register block is used as power control and gating clock

Register abbreviated name	Offset address	Description
PCGCCTL	E00h	Power and Clock Gating Control Register

13.3 Register Description

13.3.1 Register access characteristics

During the below description of register, one column of access characteristics are used to mark the read and write characteristics of these registers. The following contents will list the specific meaning of these access characteristics.

Read Only (RO)	Read only
Write Only(WO)	Write only
Read and Write(R_W)	Readable and writable
Read, Write, and Self Clear(R_W_SC)	Readable and writable; the controller can self clear, and clearing conditions have been explained in each field below in detail.
Read, Write, Self Set and Self Clear (R_W_SS_SC)	Readable and writable; the controller can self set and clear, and setting and clearing conditions have been explained in each domain below in detail.
Read, Self Set, and Write Clear R_SS_WC	Readable; OTG controller can self set the bit; when the software writes 1 to the bit and complete clearing, no effect will be generated by writing 0 to this bit. Conditions for setting OTG bit has been explained in each domain below in detail.
Read, Write Set, and Self	Readable; OTG controller can write 1 to this bit and completes bit

Clear (R_WS_SC)	setting; when the software self clears, the software can't clear. Namely, no effect will be generated by writing 1 to this bit. Conditions for OTG clearing have been explained in each domain below in detail.
Read, Self Set, and Self Clear or Write Clear (R_SS_SC_WC)	Readable; OTG controller can self set and clear; when the software writes 1 to the bit and completes clearing, no effect will be generated by writing 0 to this bit. OTG specific bit setting and clearing conditions are explained in each domain below in detail.

13.3.2 Global register

No matter OTG operates in host mode or Device mode, this register block can be accessed. When the OTG converts from one operating mode to another, it's unnecessary to instantiate these registers again.

Control and status register (GOTGCTL)
Offset address: 000h
OTG control and status register (GOTGCTL) controls OTG function and reflect its status.

file	Note	Operating mode	Reset value	Access characteristics
31:21	Reserved file	Host; Device		RO
20	OTG version	Host;	1'b0	Rw
	●1'b0: Version 1.3; this version OTG supports the SRP of Data line pulsing and VBus pulsing. ●1'b1: Version 2.0; this version OTG only supports the SRP of Data line pulsing.	Device		
19	B-session valid(BSesVld) specifies the transceiver status in device mode. ●1'b0: B-session illegal ●1'b1: B-session legitimate In OTG mode, this bit is used to decide whether the device has been connected.	Device only	1'b1	RO
18	ssesion valid(ASesVld) specifies the status of transceiver in host mode. ●1'b0: A-session illegal ●1'b1: A-session legitimate In device mode, this bit is reserved.	Host only	1'b0	RO
17	Long/ShortDebounceTime (DbncTime) specifies one debounce time finding the connection ●1'b0: long debounce time is used as physical connection (100ms + 2.5us) ●1'b1: short debounce time, used as soft connection (2.5us)	Host only	1'b0	RO
16	Connector ID status In a connection event, it indicates the ID status ●1'b0: OTG working in the mode of Device A ●1'b1: OTG working in the mode of Device B	Host ; Device	1'b1	RO
15:12	Reserved domain	Host; Device		RO
11	Device HNP enable bit (DevHNPEn) ●1'b0: HNP disable ●1'b1: HNP enable	Device Only	1'b0	R_W
10	Host Set HNP enable bit	Host only	1'b0	R_W

	●1'b0: Host Set HNP isn't enabled ●1'b1: Host Set HNP enable			
9	HNP request The software sets the bit and sends a HNP request to host. When the bit of GOTGINT.HstNegSucStsChng is set, this software is cleared by writing 0 to the bit. When the bit of HstNegSucStsChng is 0, OTG controller clears the bit. ●1'b0: No HNP request ●1'b1: HNP request	Device Only	1'b0	R_W
8	HostNegotiationSuccess (HstNegScs) When the host is exchanged (Host Negotiation), OTG controller asserts the bit. ●1'b0: host negotiation failure ●1'b1: host negotiation success	Device only	1'b0	RO
7	B-Peripheral Session Valid value (BvalidOvVal) When the bit of GOTGCTL.BvalidOvEn is set, the bit of BValidOvVal is used reset Bvalid signal. ¡ñ1'b0: When GOTGCTL.BvalidOvEn = 1, the value of Bvalid signal is 0; ●1'b1: When GOTGCTL.BvalidOvEn= 1, the value of Bvalid signal is 1;	Device only	1'b0	R_W
6	B-Peripheral Session Valid reset enable (BvalidOvEn) This bit is used to make the software override Bvalid signal by GOTGCTL.BValidOvVal bit. ●1'b1: the Bvalid signal value received from PHY is reset by BvalidOvVal. ●1'b0: Bvalid signal reset function is disabled, and the Bvalid signal used by OTG controller is namely the value received from PHY.	Device only	1'b0	R_W
5	A-Peripheral Session Valid reset value (AvalidOvVal) When the bit of GOTGCTL.AvalidOvEn is set, the bit of AValidOvVal is used reset Avalid signal. ●1'b0: When GOTGCTL.AvalidOvEn = 1, the value of Avalid signal is 0; ●1'b1: When GOTGCTL.AvalidOvEn= 1, the value of Avalid signal is 1;	Host only	1'b0	R_W
4	A-Peripheral Session Valid reset enable (AvalidOvEn) is used to make the software override Avalid signal Bvalid signal by GOTGCTL.AValidOvVal bit. ●1'b1: the Avalid signal value received from PHY is reset by AvalidOvVal. ●1'b0: Avalid signal reset function is disabled, and the Avalid signal used by OTG controller is namely the value received from PHY.	Host only	1'b0	R_W
3	VBUS Valid reset value (VbvalidOvVal)	Host only	1'b0	R_W

	When the bit of GOTGCTL.VbalidOvEn is set, the bit of VbalidOvVal is used reset vbus valid signal. ●1'b0: When GOTGCTL.VbalidOvEn = 1, the value of vbus valid signal is 0; ●1'b1: When GOTGCTL. VbalidOvEn = 1, the value of vbus valid signal is 1;			
2	VBUS Valid reset enable (AvalidOvEn) This bit is used to enable the software to override Bvalid signal by GOTGCTL.BbValidOvVal bit. ●1'b1: The vbus valid signal received from PHY is reset by VbvalidOvVal. ●1'b0: vbus valid signal reset function is disabled, and the value of vbus valid signal used by OTG controller, namely, the value received from PHY	Host only	1'b0	R_W
1	Session Request (SesReq) The software sends a session request through setting the SesReq Bit in USB bus. When the bit of Host Negotiation Success Status Change in OTG interrupt controller is set, the software is cleared by writing 0 to the bit. When the bit of HstNegSucStsChng is 0, OTG controller clears the bit. ●1'b0: No session request ●1'b1: Session request	Device only	1'b0	R_W
0	Session Request (SesReq) ●1'b0: Session request failure ●1'b1: Session request success	Device only	1'b0	R_W

Interrupt register (GOTGINT)
Offset address: 004h

Field	Note	Operating mode	Reset value	Access characteristics
31:20	Reserved field	Host; Device		RO
19	Debounce Done (DbnceDone) After the debounce in device connection is finished, OTG controller asserts the bit. After the application notices this interrupt, USB reset operation starts.	Host only	1'b0	R_SS_WC
18	A device timeout change (ADevTOUTChg) When A device waits for B device connection overtime, OTG controller asserts the bit	Host; Device	1'b0	R_SS_WC
17	detects the Host Negotiation (HstNegDet): After the Host Negotiation Request is found in bus, OTG controller asserts this bit.	Host; Device	1'b0	R_SS_WC
16:10	Reserved domain	Host and Device		RO
9	HstNegSucStsChng: Host Negotiation Successful Status Change. When the host negotiation request in bus succeeds or fails,	Host and Device	1'b0	R_SS_W C

	OTG controller will assert this bit. The software can determine whether the host negotiation succeeds by searching GOTGCTL.HstNegSus.			
8	Session request successful status change (SesReqSusStsChng) Session Request Success Status Change When the session request in USB bus succeeds or fails, OTG controller asserts this bit. The software can determine whether the session request succeeds by searching GOTGCTL.SesReqScs.	Host and Device	1'b0	R_SS_W C
7:3	Reserved domain	Host and Device	1'b0	RO
2	Session end detect (SesEndDet): Session End Detected When utmisrp_bvalid signal is pulled down, OTG controller asserts this bit.	Device	1'b0	R_SS_W C
1:0	Reserved domain	Host and Device		RO

AHB configuration register (GAHBCFG)

Offset address: 008h

This register is used to configure OTG controller in case of power on or change in operating mode, the configured contents mainly include system parameters related to AHB. After the initial configuration, the value of this register can't be modified. No matter the transaction is initiated in AHB bus or USB bus, this register needs reconfiguring.

Field	Note	Operating mode	Reset value	Access characteristics
31:23	Reserved domain	Host; Device		RO
22	Notify All DMA Write Transactions (NotiAllDmaWrit): NotifyAllDma Write Transactions It's used to enable DMA Done function of all DMA write transactions (to endpoint/Channel). Only when the bit of GAHBCFG.RemMemSupp is 1'b1, this bit is significant. ●1'b1: For all DMA write transactions, OTG controller must assert dma_req, int_dma_done, chep_last_transact and chep_number signals in AHB bus. In order to finish certain channel/endpoint transmission, OTG controller needs to wait for the sys_dma_done signal of all write transactions. ●1'b0: only for the last transaction in write transaction, will OTG controller assert int_dma_done signal. Similarly, in order to finish certain channel/endpoint transmission, OTG controller needs to wait for the sys_dma_done signal of that DMA write transactions.	Host; Device	1'b0	R_W
21	RemoteMemorySupport (RemMemSupp) Enable the DMA write transfer wait system DMA DONE signal function ●1'b1: When OTG DMA starts the	Host and Device	1'b0	R_W

	transfer towards the external memory space, the output signal int_dma_req is asserted. When this transfer is finished, OTG controller asserts int_dma_done signal to indicate that the DMA write from OTG controller is finished. Then, OTG controller waits for the sys_dma_done signal from system, so as to complete certain channel/endpoint data transfer. ● It's unnecessary to assert int_dma_req and int_dma_done signals; once DMA write transfer is finished, XferComp interrupts and OTG controller continues operating. It's unnecessary to wait for sys_dma_done signal to finish data transfer.			
8	PTxFIFOEmpLvl: periodic TxFIFO Empty Level indicates that the when the periodic TxFIFO empty interrupt bit (GINTSTS.PTxFEMp) is asserted. The bit is only used in slave mode. ●1'b0: GINTSTS.PTxFEMp interrupt bit indicates when the periodic TxFIFO is half empty; ●1'b1: GINTSTS.PTxFEMp interrupt bit indicates that the periodic TxFIFO is fully empty	Host only	1'b0	R_W
7	NPTxFIFOEmpLvl: Non-periodic TxFIFO Empty Level is used in slave mode. It indicates when the TxFIFO empty interrupt bit of IN endpoint is asserted. Host mode: ●1'b0: GINTSTS.PTxFEMp interrupt bit indicates the non-periodic TxFIFO half empty; ●1'b1: GINTSTS.PTxFEMp interrupt bit indicates the non-periodic TxFIFO fully empty; Device mode: ●1'b0: DIEPINTn.TxFEmp interrupt bit indicates the TxFIFO half empty of IN endpoint; ●1'b1: DIEPINTn.TxFEmp interrupt bit indicates the TxFIFO fully empty of IN endpoint;	Host and device	1'b0	R_W
6	Reserved domain	Host; Device		RO
5	DMA enable (DMAEn) ●1'b0: OTG working in Slave mode ●1'b1: OTG working in DMA mode	Host; Device	1'b0	R_W
4:1	Burst length (HBstLen) Burst type of AHB Master ●4'b0000: Single ●4'b0001: INCR ●4'b0000: INCR4 ●4'b0000: INCR8 ●4'b0000: INCR16 Others: Reserved	Host; Device	4'b0	R_W

0	Global interrupt mask (GlblIntrMsk) For software interrupt mask No matter whether the bit is asserted, OTG controller always updates the interrupt status register. ●1'b0: Interruption is invisible to software ●1'b0: Interruption is visible to software	Host; Device	1'b0	R_W

USB configuration register (GUSBCFG)

Offset address: 00Ch

This register is used to configure OTG controller in case of power on or change in operating mode, the configured contents mainly include parameters related to USB and USB-PHY. No matter the transaction is initiated in AHB bus or USB bus, this register needs reconfiguring. After the initial configuration, the value of this register can't be modified.

Field	Note	Operating mode	Reset value	Access characteristics
31	Corrupt Tx package () Only for debugging, not writable 1	Host; Device	1'b0	WO
30	Force device register (ForceDevMod) Writing 1 indicates that the OTG controller operates in device mode, regardless the value of utmiotg_iddig input pin. ●1'b0: Normal operating mode ●1'b1: Enforcement device mode After 1 is written to this bit, the software must wait for the effective time of at least 25ms. In the simulation environment in scale down mode, 500us is enough.	Host; Device	1'b0	R_W
29	If the Force Host Mode (ForceHostMod) writes 1, it indicates that the OTG controller will work in Host mode, regardless the value of utmiotg_iddig input pin. ●1'b0: Normal operating mode ●1'b1: Enforcement host mode After 1 is written to this bit, the software must wait for the effective time of at least 25ms. In the simulation environment in scale down mode, 500us is enough.	Host; Device	1'b0	R_W
28	Tx End Delay (TxEndDelay) Write 1, and enable TxEndDelay timer ●1'b0: Normal mode ●1'b1: Introduce Tx end delay timer	Device only	1'b0	R_W
27: 23	Reserved	Host; Device		RO
22	TermSelDLinePulsing select (TermSelDLPulse) It's used in SRP process to select utmi_termselect data line pulse. ●1'b0: It uses utmi_txvalid data line pulse (default) ●1'b1: It uses utmi_termselect data line pulse	Device	1'b0	R_W
21: 16	Reserved	Host; Device		RO
15	PHY low power clock select (PhyLpwClkSel) Choose to use 480MHz or 48Mhz (low power) PHY mode. In FS and LS modes, PHY always operate at 48MHz to save power.	Host; Device	1'b0	R_W

	●1'b0: 480MHz internal PLL clock ●1'b1: 48MHz external clock			
14	Reserved bit	Host; Device		RO
13:10	USB cycle time (USBTrdTime): USB Turnaround Time Sets the cycle time of PHY clock bit unit It specifies MAC request PFC (data FIFO controller) to clear the response time of obtaining data in data FIFO. Its value must be set as follows: ●4'h5: When MAC interface is the 16bit UTM+ ●4'h6: When MAC interface is the 16bit UTM+	Device	4'h5	R_W
9	HNP-Capable(HNPCap) The software uses this to control the HNP function of OTG controller. ●1'b0: Unavailable HNP function ●1'b0: Available HNP function Note: if the HNP function is disabled by software, the corresponding OTG signal of PHY domain must be fixed as the decided value (?)	Host, Device	1'b0	R_W
8	SRP-Capable(SRPCap) The software uses this to control the SRP function of OTG controller. ●1'b0: Unavailable SRP function ●1'b0: Available SRP function Note: if the SRP function is disabled by software, the corresponding OTG signal of PHY domain must be fixed as the decided value	Host; Device	1'b0	R_W
7: 4	Reserved bit	Host; Device		RO
3	PHY interface (PHYIf) It's used to configure the interface of UTMI+PHY. ●1'b0: 8bits ●1'b1: 16bits If ULPI interface is selected, only 8bits can be set.	Host; Device	Configura ble	RO
2:0	HS timeout calibration (TOutCal): HS Timeout The calibration unit is a PHY clock. It's used to correct the timeout between packets caused by PHY. Different PHY introducing different delay. For HS, the time-out value of USB standard is 736 -816 bit times; the software must set this domain based on enumerating speed. The bits time of each PHY clock is explained as follows: HS: ● One 30MHz PHY clock = 16bit times ● One 60MHz PHY clock = 16bit times	Host; Device	3'h0	R_W

Reset register (GRSTCTL)
Offset address: 010h

Field	Note	Operating mode	Reset value	Access characteristics
31	.AHB Master Idle(AHBIdle) It indicates that AHB Master state machine is in IDLE state.	Host; Device	1'b1	RO
30	DMA request signal (DMAReq) It indicates that there is a DMA request in bus;	Host; Device	1'b0	RO
29:11	Reserved domain	Host;		RO

		Device		
10:6	TxFIFO number (TxFNum) Debugging use indication must use the FIFO signal cleared by TxFIFO Flus. Only after TxFIFO bit is cleared by controller, can TxFNum be changed. ●5'h0: -Clear non-periodic TxFIFO in –host mode -Clear TxFIFO 0 in –device mode ●5'h1: -Clear periodic TxFIFO in host mode -Clear TxFIFO 0 in –device mode ●5'h2: -Clear TxFIFO 0 in –device mode ●5'h3: -Clear TxFIFO 0 in –device mode … ●5'H10: Clear all TxFIFOs (no matter in host mode or device mode)	Host; Device	5'h0	R_W
5	TxFIFO clear (TxFFlsh) Is used to select and clear one or all TxFIFOs. But this operation can't be performed when the transaction is under progress. Only when the software confirms that OTG controller doesn't read or write TxFIFO, can this bit be written. Acknowledged method is as follows: Read –NAK valid interrupt can make sure OTG controller doesn't read FIFO; Write -GRSTCTL.AHBIdle can make sure OTG controller doesn't write FIFO FIFO clear operations can be used in the following circumstances. For example, FIFO needs to reset or convert in share FIFO mode and dedicated FIFO mode, and disables certain device endpoint. Only after the software must wait for OTG controller to clear this bit, can other operations be continued. It may take 8 hours, and use the slower clock between phy_clk and hclk.	Host; Device	1'b0	R_WS_SC
4	RxFIFO flash (RxFFlsh) It's used to clear the entire RxFIFO, and this operation can't be conducted in case of transaction under progress. Only when the software confirms that OTG controller doesn't read or write RxFIFO, can this bit be written. Only after the software must wait for OTG controller to clear this bit, can other operations be continued. It may take 8 hours, and use the slower clock between phy_clk and hclk.	Host; Device	1'b0	R_WS_SC
3	Reserved bit	Host; Device		RO
2	Host Frame Counter Reset (FrmCntrRst) The software resets the frame number in OTG	Host	1'b0	R_WS_SC

	controller by this bit. Once the frame number is reset, the frame number of SOF sent by next OTG controller is 0.			
1	Reserved domain	Host; Device		RO
0	OTG controller soft restart The contents of resetting hclk and phy_clock clock domains are as follows: ● Clear all interrupts and CSR registers except the following -PCGCCTL.RstPdwn -PCGCCTL.GateHclk -PCGCCTL.PwrClmp -GUSBCFG.DDRSel -GUSBCFG.PHYSel -GUSBCFG.FSIntf -GUSBCFG.ULPI_UTMI_Sel -GUSBCFG.PHYIf -HCFG>FSLSPclkSel -DCFG.DevSpd -GGPIO -GPWRDN -GADPCTL ● Status machines of all modules (except AHB Slave unit) are set to IDLE status; clear all TxFIFOs and RxFIFOs ● After completing the data of the last AHB transfer, all AHB Master transactions are ended at once. An immediate end to all USB transaction ¡ñ PMU module (power management unit) won't be reset, and the software can soft reset OTG controller in any time. This bit is self cleared, namely, the controller will self clear after all necessary logics are reset. Based on different states of controllers, this will spend several hours. Once this bit is cleared, only after waiting for three PHY clocks, can PHY domain operate (sync delay). Before the software starts any action, the AHBIdle bit must be maintained at 1.	Host; Device	1'b0	R_WS_SC

Interrupt register (GITTSTS)
Offset address: 014h

Field	Note	Operating mode	Reset value	Access characteristics
31	System recovery / remote wake-up interrupt (WkUpInt):Resume/Remote Wakeup Detected Interrupt The wakeup interrupt in suspended (L2) state. ● Device mode: only when the wakeup operation started by Host is found in USB bus, can this interrupt generate. ● Host mode: only when the wakeup operation started	Host; Device	1'b0	R_SS_WC

	by device is found in USB bus, can this interrupt generate.			
30	SessionRequest/New Session Detected Interrupt ● In Host mode, when the session request from device is found, the bit is set to 1. ●In device mode, when the utmisrp_bvalid signal is pulled high, the bit is set to 1.	Host; Device	1'b0	R_SS_WC
29	Disconnect interrupt (DisconnInt) When the device is disconnected, the bit is set to 1.	Host	1'b0	R_SS_WC
28	Connector ID Status Change (ConIDStsChng) When the connector ID status changes, the bit is set 1.	Host; Device	1'b1	R_SS_WC
27	Reserved bit	Host; Device		RO
26	Periodic TxFIFO (PTxFEmp) When the periodic TxFIFO is half empty or full empty, and there is at least one request in cycle request queue, this bit is set 1, and whether it's set to 1 in half empty or full empty is decided by GAHBCFG.PTxFEmpLvl.	Host	1'b1	RO
25	Host Channels Interrupt (HChInt) In Host mode, when there is a pending interrupt in some channel of OTG controller, it's set 1. The software must read HAINT register to determine the unprocessed interrupt channel number, and then read the corresponding HCINTn register to determine reasons for the interrupt. In order to clear this bit, the software must clear the corresponding status bit in HCINTn register.	Host	1'b0	RO
24	Host port interrupt (PrtInt) In Host mode, if some port status of OTG controller changes, it's set to 1. The software must read HPRT register to determine the real reason for the interrupt. In order to clear this bit, the software must clear the corresponding status bit in HPRT register.	Host	1'b0	RO
23	ResetDet: Reset Detected Interrupt In device mode, when the OTG controller in suspended state sends the next reset operation, the bit is set to 1. Only when the OTG controller is in device mode, and works in partial Power-down, or gating suspended status, can it is valid. When the OTG controller operates in Hibernation suspended state, the bit is significant.	Device	1'b0	R_SS_WC
22	FetSusp: Data Fetch Suspended Valid only in DMA mode. When TxFIFO or request queue has no space, OTG will stop and obtain data for IN endpoint, and the bit is set to 1. In the endpoint mismatching algorithm, the software uses this interrupt	Device	1'b0	R_SS_WC
21	Incomplete periodic transfer (incomplIP) In Host mode, when one incomplete periodic transaction is still waiting processing within the current frame time, the bit is set 1. In device mode, the incomplete real-time OUT transmission, if within the current frame time, there is at least one incomplete transmission in a real-time OUT	Host Device	1'b0	R_SS_W C

	endpoint, the bit is set to 1. And EOPF bit			
20	Incomplete real-time IN transmission (incomplSOIN) If within the current frame time, there is at least one incomplete transmission in a real-time IN endpoint, the bit is set to 1. And EOPE bit	Device	1'b0	R_SS_WC
19	OUT endpoint interrupt (OEPInt) When there is one pending interrupt in OUT endpoint, the bit of OTG controller is set to 1. The software must read DAINT register to determine which endpoint has the pending interrupt, and then read DOEPINTn register to determine the causes of this interrupt. In order to clear this bit, the software must clear the corresponding status bit in DOEPINTn register.	Device	1'b0	RO
18	IN endpoint (IEPInt) When there is one pending interrupt in IN endpoint, the bit of OTG controller is set to 1. The software must read DAINT register to determine which endpoint has the pending interrupt, and then read DOEPINTn register to determine the causes of this interrupt. In order to clear this bit, the software must clear the corresponding status bit in DOEPINTn register.	Device	1'b0	RO
17	Reserved bit	Host; Device		RO
16	Reserved bit	Host; Device		RO
15	Periodic frame end (EOPF) When within the current frame time, the threshold pointed by DCFG.PerFrInt is reached, the bit is set 1.	Device	1'b0	R_SS_WC
14	Real-time OUT packet drop (ISOOutDrop) If RxFIFO doesn't have enough space for real-time OUT endpoint to store the maximum package size packet, the OTG controller can't write one real-time OUT packet to FxFIFO. In case of such circumstance, the bit is set to 1.	Device	1'b0	R_SS_W C
13	EnumDone : Enumeration done When the speed enumeration ends, the bit is set 1. The software reads DSTS register, and obtains the specific enumeration speed.	Device	1'b0	R_SS_WC
12	USB reset (USBRst) When there is one reset operation in USB bus, the bit is set to 1.	Device	1'b0	R_SS_WC
11	USB suspend (USBSusp) When the OTG controller detects one suspended operation in USB bus, the bit is set. If within a longer time, there is no activity in utmi_linestate signal line, OTG controller enters into the suspended state.	Device	1'b0	R_SS_WC
10	Early Suspend(ErlySusp) When the USB is detected to enter into idle state for over 3ms, the OTG controller sets the bit to 1.	Device	1'b0	R_SS_WC
9:8	Reserved bit	Host; Device		RO
7	Global OUT NAK Effective (GOUTNakEff) When it's effective after the software sets the bit of DCTL.SGOUTNak, the bit is set to 1. Clear this bit	Device	1'b0	RO

	by clearing 0 DCTL.SGOUTNak bit.			
6	Global IN non-periodic NAK effective (GINNakEff) When it's effective after the software sets the bit of DCTL.SGNPInNak, the bit is set to 1 Clear this bit by clearing 0 DCTL. SGNPInNak bit.	Device	1'b0	RO
5	Reserved bit	Host; Device		RO
4	RxFIFO non-empty (RxFLvl) When there is at least a packet in RxFIFO, the bit is set to 1.	Host; Device1	1'b0	RO
3	Start of frame (Sof) In Host mode, when SOF transmits in USB bus, the OTG controller sets the bit to 1. The software writes 1 and clears this bit. In Device mode, when OTG controller receives SOFT token, the bit is set to 1. The software can obtain the current frame number by reading Device status register.	Host; Device	1'b0	R_SS_WC
2	OTG interrupt (OTGInt) It's set to 1, and indicates that the OTG protocol transaction occurs. The software can read GOTGINT register to determine the causes of interrupt. In order to clear this bit, the software must clear the corresponding status bit of GOTGINT register.	Host; Device	1'b0	RO
1	Mode mismatch interrupt (ModeMis) When the software tries to perform the next operation, the bit is set to 1. ¡ñ When OTG operates in device mode, it tries to access the register in host mode. When OTG operates in host mode, it tries to access the register in device mode.	Host; Device	1'b0	R_SS_WC
0	Current operating mode (CurMod) It indicates the operating mode of the current OTG controller. ●1'b0: device mode ●1'b1: host mode	Host; Device	1'b0	RO

Interrupt mask register (GINTMSK)

Offset address: 018h

This register and GINTSTS register are used at the same time. When some interrupt is masked, this interrupt will not be seen by software. Of course, the bit corresponding to GINTSTS is still set.

Field	Note	Operating mode	Reset value	Access characteristics
31	System recovery/remote wakeup interrupt mask bit (WkUpInt):Resume/RemoteWakeup Detected Interrupt Mask	Host; Device	1'b0	R_SS_WC
30	SessionRequest/New Session Detected Interrupt (SessReqIntMsk): Session Request/New Reset Detected Interrupt Mask	Host; Device	1'b0	R_SS_WC
29	DisconnIntMsk (disconnect interrupt mask)	Host	1'b0	R_SS_WC
28	Connector ID Status Change (ConIDStsChngMsk)	Host; Device	1'b1	R_SS_WC
27	Reserved bit	Host; Device		RO
26	Periodic TxFIFO Empty Mask (PTxFEmpMsk)	Host	1'b1	RO

25	Host Channels Interrupt mask (HChIntMsk)	Host	1'b0	RO
24	Host port interrupt mask (PrtIntMsk)	Host	1'b0	RO
23	ResetDetMsk: Reset Detected Interrupt Mask	Device	1'b0	R_SS_WC
22	FetSuspMsk: Data Fetch Suspended Mask	Device	1'b0	R_SS_WC
21	Incomplete periodic transfer mask (incomplIPMsk) Incomplete real-time OUT transmission mask (incomplSOOUTMsk)	Host Device	1'b0	R_SS_WC
20	Incomplete real-time IN transmission mask bit (incomplSOINMsk)	Device	1'b0	R_SS_WC
19	OUT endpoint interrupt mask (OEPIntMsk)	Device	1'b0	RO
18	IN endpoint interrupt mask (IEPIntMsk)	Device	1'b0	RO
17:16	Reserved bit	Host; Device		RO
15	End of Periodic frame mask (EOPFMsk)	Device	1'b0	R_SS_WC
14	Read-time OUT packet Drop Mask (ISOOutDropMsk)	Device	1'b0	R_SS_WC
13	Enumeration done mask (EnumDoneMsk): Enumeration Mask	Device	1'b0	R_SS_WC
12	USB reset mask (USBRstMsk)	Device	1'b0	R_SS_WC
11	USB suspended mask (USBSuspMsk)	Device	1'b0	R_SS_WC
10	Early Suspend mask (ErlySuspMsk)	Device	1'b0	R_SS_WC
9:8	Reserved bit	Host; Device		RO
7	Global OUTNAK valid mask (GOUTNakEffMsk)	Device	1'b0	RO
6	Global IN periodic NAK effective mask (GINNakEffMsk)	Device	1'b0	RO
5	Reserved bit	Host; Device		RO
4	RxFIFO non-periodic mask (RxFLvlMsk)	Host; Device1	1'b0	RO
3	Start of Frame Mask Bit (SofMsk)	Host; Device	1'b0	R_SS_WC
2	OTG interrupt mask (OTGIntMsk)	Host; Device	1'b0	RO
1	Mode mismatching interrupt mask (ModeMisMsk)	Host; Device	1'b0	R_SS_WC
0	Current Operating Mode Bit (CurMod)	Host; Device	1'b0	RO

Receive status debugging register/status read and pop register (GRXSTSR/GRXSTSP)

Read offset address: 01Ch

Pop offset address: 020h

The read operation of receive status debugging register is the first option of RxFIFO. The read operation of status read and pop register will pop the first option of RxFIFO.

The contents of receive status register have different explanations in host mode and device mode. If RxFIFO is empty, OTG controller will ignore the read and pop operations of this register, and return 32'h0000_0000. When the bit of GINTSTS.RxFLvl is 1, the software can only pop the receive Stastus FIFO.

NOTES: in different operating modes of OTG, all domains of this register have different explanations.

Host mode

Field	Note	Reset value	Access characteristics

31:21	Reserved domain	1	RO
20:17	Package status (PktSts) Indicate the status of the received packet: ●4'b0010: IN data packet is received ●4'b0011: IN transmission end (triggered interrupt) ●4'b0101: Data toggle error (triggered interrupt) ●4'b0111: Channel halt (triggered interrupt) ●Others: reserved	4'b0	RO
16:15	Data PID (DPID) Indicate received packet data PID ●2'b00:DATA0 ●2'b10:DATA1 ●2'b01:DATA2 ●2'b11:MDATA	2'b0	RO
14:4	Number of bytes (BCnt) Indicate the byte number o the received IN data packet	11'h0	RO
3:0	Channel number (ChNum) Indicate the channel number of the currently received data packet	4'h0	RO

Device mode

Field	Note	Reset value	Access characteristics
31:25	Reserved domain		RO
24:21	Frame number (FN) The lowest 4 bits of the frame number of the received packet frame Only when it supports the real-time OUT endpoint, is this domain effective.	4'h0	RO
20:17	Package status (PktSts) Indicate the status of the received packet: ●4'b0001: Global OUT NAK (triggered interrupts) ●4'b0010: OUT data packet is received ●4'b0011: OUT transmission end (triggered interrupts) ●4'b0100: SETUP transaction end (triggered interrupt) ●4'b0110: SETUP data packet is received ●Others: reserved	4'b0	RO
16:15	Data PID (DPID) Indicate the data PID of the received OUT packet ●2'b00:DATA0 ●2'b10:DATA1 ●2'b01:DATA2 ●2'b11:MDATA	2'b0	RO
14:4	Number of bytes (BCnt) Indicate the byte number o the received IN data packet	11'h0	RO
3:0	Endpoint number (EPNum) Indicate the endpoint number of the currently received data packet	4'h0	RO

RxFIFO capacity register (GRXFSIZ)

Read offset address: 024h

The RAM size of RxFIFO which the software uses the register to allocate

Field	Note	Reset value	Access characteristics

31:16	Reserved domain		RO
15:0	RxFIFO depth (RxFDep) A 32-bits word as a unit. ●The minimum value is 16 ●The maximum value is 32768	533	R_W

Non-periodic TxFIFO capacity register (GNPTXFSIZ)
Read offset address: 028h
The RAM size and starting address which the software uses the register to allocate to non-periodic TxFIFO
Note: no matter the OTG is in host operating mode or device operating mode, the register has different explanations.
In Host mode

Field	Note	Reset value	Access characteristics
31:16	Non-periodic TxFIFO depth (NPTxDep)	256	R_W
	A 32-bits word as a unit. ●The minimum value is 16 ●The maximum value is 32768		
15:0	Non-periodic TxRAM starting address (NPTxStAddr)	533	R_W

In Device mode

Field	Note	Reset value	Access characteristics
31:16	TxFIFO0 Depth of IN endpoint It is effective only in Device mode and OTG_EN_DED_TX_FIFO = 1 ●The minimum value is 16 ●The maximum value is 32768	32	R_W
15:0	FIFO0 TxRAM initial address of IN endpoint	533	R_W

Synopsys ID register (GSNPSID)
Read offset address: 040h
The version number containing OTG controller

Field	Note	Reset value	Access characteristics
31: 0	Synopsys ID (SynopsysID) OTG controller version number	32'h4F54	RO

User HW Config1 register
Read offset address: 044h
User's hardware configuration register 2, specifying the endpont direction

Field	Note	Reset value	Access characteristics
31: 14	Reserved domain	18'b0	RO

13: 0	Bits[13:12]:endpoint 6 direction Bits [11:10]: endpoint 5 direction Bits[9:8]:endpoint 4 direction Bits[7:6]:endpoint 3 direction Bits[5:4]:endpoint 2 direction Bits[3:2]:endpoint 1 direction Bits[1:0]:endpoint 0 direction ●2'b00: Bidirectional endpoint ●2'b01: IN endpoint ●2'b10: OUT endpoint ●2'b11: Reserved	14'b0	RO

User HW Config2 register
Read offset address: 048h
User's hardware configuration register 2

Field	Note	Reset value	Access characteristics
[31:26]	Reserved domain	6'b0	RO
25: 24	Aperiodic request queue depth ●2'b00: 2 ●2'b01: 4 ●2'b10: 8 ●2'b11: 16	2'b10	RO
23: 22	Non-periodic request queue depth ●2'b00: 2 ●2'b01: 4 ●2'b10: 8 ●2'b11: 16	2'b10	RO
21	Reserved domain		RO
20	Enable multiple processors interrupt ●1'b0: No ●1’b1: Yes	1'b0	RO
19	Enable dynamic FIFO size ●1'b0: No ●1’b1: Yes	1'b1	RO
18	Enable periodic OUT channel ●1'b0: No ●1’b1: Yes	1'b1	RO
17:14	The number of Channel in the Host mode	4'd12	RO
13:10	The number of endpoint in device mode, expect endpoint 0	4'd6	RO
9: 8	Full speed PHY interface type ●2'b00: none ●2'b01: FS has a dedicated pin ●2'b10: Shared with UTMI + ● 2'b11: shared with ULPI	2'b0	RO
7:6	HS PHY interface type ●2'b00: none ●2'b01: UTMI+ ●2'b10: ULPI ●2'b11: UTMI + and ULPI	2'b0	RO
5	PTP (point-to-point) ●1'b0: No	1'b1	RO

	●1’b1: Yes		
4: 3	Architecture ●2'b00: Only as slave unit ●2'b01: External DMA ●2'b10: Embedded DMA ●2'b11: Reserved	2'b10	RO
2:0	Operating mode ●3'b000: support the OTG of HNP and SRP (host and device) ●3'b001: only support the OTG of SRP (host and device) ●3'b010: not support the OTG of HNP and SRP (host and device) ●3'b011:support the device of SRP ●3'b100: the device of non-OTG ●3'b101: support the device of SRP ●3'b110: the host of non-OTG ●Others: reserved	3'b000	RO

User HW Config3 register
Read offset address: 04Ch
User's hardware configuration register 3

Field	Note	Reset value	Access characteristics
[31:16]	DFIFO depth ●The minimum value is 32 ●The maximum value is 32768	16'd3072	RO
15	OTG_ENABLE_LPM Specify whether the OTG supports LPM mode ●1'b0: No ●1’b1: Yes	1'b0	RO
14	OTG_BC_SUPPOT Specify whether to support USB charging function ●1'b0: No ●1’b1: Yes	1'b0	RO
13	OTG_ENABLE_HSIC Specify whether to support HSIC ●1'b0: No ●1’b1: Yes	1'b0	RO
12	OTG_ADP_SUPPORT Specify whether to support ADP ●1'b0: No ●1’b1: Yes	1'b0	RO
11	OTG_SYNC_RESET_TYPE Specify whether to support synchronous reset ●1'b0: No ●1’b1: Yes	1'b0	RO
10	Remove some unnecessary features (OptFeature) ● 1’b0: No ● 1’b1: Yes	1'b1	RO
9	Whether to support vendor control interface (VndctlSupt) The interface is used to access PHY internal register. ●1'b0: No	1'b0	RO

	● 1’b1: Yes		
8	Whether to support I2C interface (I2CIntSel) ●1'b0: No ●1’b1: Yes	1'b0	RO
7	OTG function enable (OtgEn) Specify whether to enable OTG function ●1'b0: No ●1’b1: Yes	1'b1	RO
6: 4	Packet Counters width (PktSizeWidth) Indicate the maximum number of USB controller send/ receive Packet in a transmission ●3'b000: 4bits ●3'b001: 5bits ●3'b010: 6bits ●3'b011: 7bits ●3'b100: 8bits ●3'b101: 9bits ●3'b110: 10bits ●Others: reserved	3'b110	RO
3: 0	TransferSizeCounters width(XferSizeWidth), indicate the maximum size of data transmission ●4'b0000: 11bits ●4'b0001: 12bits … ●4'b1000: 19bits Others: Reserved	4'b1000	RO

User HW Config4 register
Read offset address: 050h
User's hardware configuration register 4

Field	Note	Reset value	Access characteristics
31	Reserved		RO
30	Wether to support Scatter/Gather DMA ●1'b0: No ●1’b1: Yes	1'b1	RO
29:26	In Device mode, the number of IN endpoint, including endpoint0 (INEps) ●0: 1 IN endpoints ●1: 2 IN endpoints … ●16: 16 IN endpoints	4	RO
25	For Device In endpoint enable dedicated TxFIFO ●1'b0: No ●1’b1: Yes	1'b1	RO
24	Whether to add the de-twitter logic to session_end signal ●1'b0: No ●1’b1: Yes	1'b1	RO
23	Whether to add the de-twitter logic to b_valid signal ●1'b0: No	1'b1	RO

	●1’b1: Yes		
22	Whether to add the de-twitter logic to a_valid signal ●1'b0: No ●1’b1: Yes	1'b1	RO
21	Whether to add the de-twitter logic to vbus_valid signal ●1'b0: No ●1’b1: Yes	1'b1	RO
20	Whether to add the de-twitter logic to iddig_valid signal ●1'b0: No ●1’b1: Yes	1'b1	RO
19:16	Remove endpoint0£¬ control the number of ednpoints in device mode	4'b0	RO
15:14	UTMI + PHY data width ●2'b00: 8bits ●2'b01: 16bits ●2'b10: 8/16 bits software selectable ●2'b11: Reserved	2'b10	RO
13:7	Reserved domain		RO
6	Enable Hibernation ¡ñ1’b0: No ●1'b1: Yes	1'b0	RO
5	If AHB frequency lower than the minimum 60MHA(AhbFreq) ●1’b0: No ●1'b1: Yes	1'b0	RO
4	Whether to reduce part of the power consumption ●1’b0: No ●1'b1: Yes	1'b1	RO
3:0	Reserved field		RO

DFIFO software configuration register (GDFIFOCFG)
Read offset address: 05Ch

Field	Note	Operating mode	Reset value	Access characteristics
31:16	EPInfoBaseAddr Initial address of Endpoint controller	Host; Device	EPINFO_BASEADDR	R_W
15:0	GDFIFOCfg Dynamic configuration of DFIFO size	Host; Device	3072	R_W

Periodic TxFIFO capacity register in Host mode (GNPTXFSIZ)
Read offset address: 0100h

Field	Note	Reset value	Access characteristics
31:16	PTxFSize Periodic TxFIFO depth (NPTxDep) 32-bits word as a unit.	512	R_W

	●The minimum value is 16 ●The maximum value is 32768		
15:0	PTxFStAddr Initial address of periodic TxFIFO in Host mode	789	R_W

IN endpoint TxFIFO1 capacity register in Device mode (DIEPTXF1)
Read offset address: 0104h

Field	Note	Reset value	Access characteristics
31:16	INEPnTxFDep IN endpoint TxFIFO1 depth£¬a 32-bit word as a uint. ●The minimum value is 16 ●The maximum value is 32768	256	R_W
15:0	INEPnTxFStAddr Initial address of IN endpoint FIFO 1	565	R_W

IN endpoint TxFIFO2 capacity register in Device mode (DIEPTXF2)
Read offset address: 0108h

Field	Note	Reset value	Access characteristics
31:16	INEPnTxFDep IN endpoint TxFIFO2 depth, 32-bit word as a uint. ●The minimum value is 16 ●The maximum value is 32768	256	R_W
15:0	INEPnTxFStAddr Initial address of IN endpoint FIFO 2	821	R_W

IN endpoint TxFIFO3 capacity register in Device mode (DIEPTXF3)
Read offset address: 010Ch

Field	Note	Reset value	Access characteristics
31:16	INEPnTxFDep IN endpoint TxFIFO3 depth, 32-bit word as a uint. ●The minimum value is 16 ●The maximum value is 32768	512	R_W
15:0	INEPnTxFStAddr Initial address of IN endpoint FIFO 3	1077	R_W

13.3.3 Host mode register

This register block is only effective in Host mode, and can't be accessed in host mode.

Host mode configuration register (HCFG)
Offset address: 400h

Field	Note	Reset value	Access characteristics
31:28	Reserved domain		RO
27	ModeChTimEn Whether to enable mode changes into ready timer.	1'b0	R_W

	Decide at the end of Resume state whether to enable host controller to change 2'b10 into 00 of PHY opmode signal after waiting for 200PHY clocks ●1'b0: No ●1'b1: Yes		
26	PerSchedEna Whether to enable periodic schedule. ●1'b0: No ●1'b1: Yes	1'b0	R_W
25:24	FrListEn Frame list number of terms ●2'b00: 8 ●2'b01: 16 ●2'b00: 32 ●2'b00: 64	2'b00	R/W
23	DescDMA In Host mode, enable Scatter/gather DMA Note: after resetting, this can only be modified once. The following configurations are available: ●GAHBCFG.DMAEn = 0, HCFG.DescDMA = 0 => slave mode; ●GAHBCFG.DMAEn= 0, HCFG.DescDMA = 1 => illegal configuration; GAHBCFG.DMAEn= 1, HCFG.DescDMA = 0 => Buffered DMA mode; ●GAHBCFG.DMAEn= 0, HCFG.DescDMA = 1 => Scatter/Gather mode;	1'b0	RO
15:0	Reserved domain		RO

Host frame interval register (HFIR)

Offset address: 404h

Field	Note	Reset value	Access characteristics
31:17	Reserved field		RO
16	Reload control Does it allow the dynamic reloading into HFIR register ●1'b0: No ●1'b1: Yes	1'b0	R_W
15:0	Frame interval (FrInt) The software uses this value to determine the interval between two consecutive micro-SOFs In PHY clock bit units. Only after the bit of HPRT.PrtEnaPort is set to 1, can this bit be changed. No changes can be made after the initial configuration. 125us * (PHY clock frequency)	16'd60000	R_W

Host frame number/rest frame time register (HFNUM)

Read offset address: 408h

Field	Note	Reset value	Access characteristics
31:16	Remaining frame time It indicates the rest time of the current microFrame in	16'h0	RO

	the unit of PHY clock. When the bit is 0, the value of HFIR.FrInt is reloaded, and one new SOF is sent in USB bus		
15:0	Frame number (FrNum) In a new SOF transfer, this domain adds 1, and when reaching 16'h3FFF, it's reset to 0.	16'h3FFF	RO

Host periodic TxFIFO/Queue status register (HPTXSTS)

Offset address: 410h

Field	Note	Reset value	Access characteristics
31:24	PTxQTop The first item of periodic TxFIFO request (TOP) is used for debugging. ●Bits [31]: Odd-even frame -1'b0: Transmit in even frames -1'b1: Transmit in odd frame ●Bits [30:27]: channel number ●Bits [26:25]: type -2'b00: IN / OUT -2'b01: 0 length packet -2'b10: CSPLIT -2'b11: invalid channel command ●Bits [24]: Terminate (the last item for the selected channel)	8'h0	RO
23:16	PTxQSpcAvali Periodic Tx available request queue number of term. It indicates the number of null terms in periodic request queue, and the request queue includes IN and OUT. ●8'h0: queue full ●8'h1: 1 null terms ●8'h2: 2 null terms 。。。。 ●8'h8: 8 null terms ●Others: Reserved	8	RO
15:0	PTxFSpcAvail Periodic TxFIFO available number of term A 32-bits word as a unit. ●16'h0: FIFO full ●16'h1: 1 null terms … ●16'h200: 512 null terms	512	RO

Host interrupt register in all channels (HAINT)
Read offset address: 414h

Field	Note	Reset value	Access characteristics
31:16	Reserved domain		RO
15:0	Channel interrupt (HAINT) One bit corresponds to one channel: Bits [11]: channel 11 。。。 Bits0 : channel 0	16'h0	RO

Host All Channel Interrupt Mask Register (HAINTMSK)
Read offset address: 414h

Field	Note	Reset value	Access characteristics
31:16	Reserved field		RO
15:0	Channel Interrupt Mask (HAINTMSK) One bit corresponds to one channel: Bits [11]: channel 11 。。。 Bits 0: channel 0	16'h0	R_W

Host Port Control and Status Registers (HPRT)
Read offset address: 440h

Field	Note	Reset value	Access characteristics
31:19	Reserved field		RO
18:17	PrtSpd Port Speed ●2'b00: high speed ●2'b01: full speed ●2'b10: low speed ●2'b11: Reserved	2'b0	RO
16:13	PrtTstCtl Port test control When the software writes non-0 value to this domain, the port enters into the test mode. The corresponding Pattern occurs in port. ●4'b0000: Non-test mode 4'b0001: Test_J mode ●4'b0010: Test_K mode ●4'b0011: Test_SE0_NAK mode ●4'b0100: Test_Packet mode ●4'b0101: Test_Force mode ●Others: Reserved	4'h0	R_W
12	PrtPwr Port power supply. ●1'b0:power off ●1'b1:power on	1'b0	R_W_SC
11:10	Port Line Status(PrtLnSts) ●Bits [10]: D ●Bits [11]: D	1'b0	RO
9	Reserved		RO
8	Port reset (PrtRst)	1'b0	R_W
7	Port suspend (PrtSup)	1'b0	R_WS_SC
6	Port restoration (PrtRes)	1'b0	R_W_SS_SC
5	Port overcurrent change (PrtOvrCurrChng) When PrtOvrCurrAct changes, OTG controller sets the bit to 1	1'b0	R_SS_WC
4	Port Overcurrent Activity (PrtOvrCurrAct) ●No ●Yes	1'b0	RO
3	Port Enable Status Change (PrtEnChng) When PrtEna changes, OTG controller sets the bit to 1	1'b0	R_SS_WC

2	Port enable bit (PrtEna) ●1'b0: No ●1'b1: Yes	1'b0	R_SS_SC _WC
1	When PrtConnDet (Port connection detect) finds the device connection, it'll trigger interrupt by GINTSTS.PrtInt. Write 1 for software and clear this bit.	1'b0	R_SS_WC
0	Port connection status (PrtConnSts) ●No device is connected to this port ●Device is connected to this port	1'b0	RO

Host Channel-n characteristic register (HCCHARn)
Channel_num: 0 <= n <= 11
Read the offset address: 500h + (Channel_num * 20h)

Field	Note	Reset value	Access characteristics
31	Channel enable (ChEna) When Scatter/Gather mode is enabled, ●1'b0: Indicate the descriptor structure is not ready ●1'b1: It indicates that the descriptor structure and data buffer have been prepared, and the channel can access the descriptor When Scatter/Gather mode is disabled, ●1'b0: Channel disable ●1'b1: Channel enable	1'b0	R_WS_SC
30	Channel disable (ChDis) Even if the transmission in channel hasn't finished, the software ware can stop the data transmission and receive in this channel by setting the bit to 1. The software must wait that the endpoint valid interrupt happens, can it think the channel has been invalid.	1'b0	R_WS_SC_SS
29	Odd frames (OddFrm) The software notifies that OTG host must finish one transmission within odd micro Frame by setting the bit to 1. This domain is only valid to periodic transaction (real-time and interrupt) ●1'b0: Even frames ●1'b1: Odd frames	1'b0	R_W
28:22	Device address (DevAddr)	7'h0	R_W
21:20	MultiCount (MC) /ErrorCount(EC) When HCSPLTn.SpltEna is 1'b0, this domain indicates the number of transactions finished within each microFrame time for each periodic endpoint. For the non-periodic transmission, this domain is only used in DMA mode, and is used to specify the number of packets obtained by host for this channel before the DMA changes the arbitration. ● 2'b00: Reserved ● 2'b01: 1 transaction ● 2'b10: 2 transaction ● 2'b11: 3 transaction When CSPLTn.SpltEna is 1'b1, the domain indicates the retransmission times in case of a periodic split transaction. At least set 2'b01	2'b0	R_W
19:18	Endpoint type (EPType) ●2'b00: Control	2'b0	R_W

	●2'b01: Real time ●2'b10: Bulk ●2'b11: Interrupt		
17:16	Reserved		RO
15	Endpoint direction (EPDir) ●1'b0: OUT ●1'b1: IN	1'b0	R_W
14:11	Endpoint number	4'b0	R_W
10:0	Maximum packet size (MPS)	11'h0	R_W

Host Channel-n Split control register (HCSPLTn)
Channel_num: 0 <= n <= 11
Read offset address: 504h + (Channel_num * 20h)

Field	Note	Reset value	Access characteristics
31	Split enable	1'b0	R_W
30:17	Reserved		RO
16	Do Complete Split It indicates OTG host must finish one complete split transmission	1'b0	R_W
15:14	Transaction position (XactPos) ●2'b00; all, entire data of this transaction (Less than or equal to 188B) ●2'b01:begin, the starting data of this transaction (less than or equal to 188B) ●2'b10:Mid, the intermediate data of this transaction (less than or equal to 188B) ●2'b01: End, the end data of this transaction (less than or equal to 188B)	2'h0	R_W
13:7	Hub address (HubAddr)	7'b0	R_W
[6£°0]	Port address (PrtAddr)	7'h0	R_W

Host Channe-n interrupt register (HCINTn)
Channel_num: 0 <= n <= 11
Read offset address: 508h + (Channel_num * 20h)

Field	Note	Reset value	Access characteristics
31:14	Reserved		RO
13	Descriptor rollover interrupt (DESC_LST_ROLLIntr) Only when the Scatter/Gather DMA mode is enabled, this domain is valid. The bit is set to 1 when the descriptor list in corresponding channel rolls over. For non-Scatter/Gather DMA mode, this domain set reserves the field	1'b0	R_SS_WC
12	Excessive transaction error (XCS_XACT_ERR) When the Scatter/Gather DMA mode is enabled, this domain is valid. When three consecutive transactions go wrong, the bit is set to 1. For non-Scatter/Gather DMA mode, this domain set reserves the field	1'b0	R_SS_WC
11	BNA(buffer unavailable) interrupt (BNAIntr)	1'b0	R_SS_WC

	When the Scatter/Gather DMA mode is enabled, this domain is valid. When the descriptor access isn't prepared, the bit is set to 1. For non-Scatter/Gather DMA mode, this domain set reserves the field		
10	Data inversion error (DataTglErr)	1'b0	R_SS_WC
9	Frame overrun (FrmOvrun)	1'b0	R_SS_WC
8	Bubble error (BblErr)	1'b0	R_SS_WC
7	Transaction error (XactErr) When the error occurs in USB bus, the bit is set to 1: ●CRC verify unsuccessfully ●Time-out ●Bit stuffing error ●Wrong EOP	1'b0	R_SS_WC
6	Receive NYET handshake (NYET)	1'b0	R_SS_WC
5	Receive ACK handshake (ACK)	1'b0	R_SS_WC
4	Receive NAK handshake (NAK)	1'b0	R_SS_WC
3	Receive STALL handshake (STALL)	1'b0	R_SS_WC
2	AHB error (AHBErr)	1'b0	R_SS_WC
1	Channel halted (ChHltd) For non- Scatter/Gather DMA mode, the abnormal end of transmission caused by USB transmission error or software sets invalid request, or the bit is set to 1 in normal end. For Scatter/Gather DMA mode, if the transmission ends because of the following reasons, the bit is set to 1: ● EOL setting in descriptor ● AHB error ● Excessive transaction error ● Invalid software setting request ● Vacuole ● Stall	1'b0	R_SS_WC
0	EOT (end of transmission) For Scatter/Gather DMA mode, it indicates completing the process of the current descriptor, and the bit of the descriptor IOC is set to 1. For non- Scatter/Gather DMA mode, it indicates the completion of transmission without any error.	1'b0	R_SS_WC

Host Channel-n interrupt mask register *(HCINTMSKn)

Channel_num: 0 <= n <= 11

Read offset address: 50Ch + (Channel_num * 20h)

Field	Note	Reset value	Access characteristics
31:14	Reserved		RO
13	Descriptor rollover interrupt mask bit (DESC_LST_ROLLIntrMsk) Only when the Scatter/Gather DMA mode is enabled, this domain is valid. For non-Scatter/Gather DMA mode, this domain set reserves the field	1'b0	R_W
12	Reserved		RO
11	Reserved		RO
10	Data reverse error interrupt mask (DataTglErrMsk)	1'b0	R_W
9	Frame overrun interrupt mask (FrmOvrunMsk)	1'b0	R_W

8	Bubble error interrupt mask (BblErrMsk)	1'b0	R_W
7	Transaction error mask (XactErrMsk)	1'b0	R_W
6	Receive NYET handshake interrupt mask (NYETMsk)	1'b0	R_W
5	Receive ACK handshake interrupt mask (ACKMsk)	1'b0	R_W
4	Receive NAK handshake interrupt mask (NAKMsk)	1'b0	R_W
3	Receive STALL handshake interrupt mask (STALLMsk)	1'b0	R_W
2	AHB error interrupt mask (AHBErrMsk)	1'b0	R_W
1	Channel halted interrupt mask (ChHltdMsk)	1'b0	R_W
0	Transfer complete interrupt mask (XferComplMsk)	1'b0	R_W

Host Channel-n transfer size register (HCTSIZn)

Channel_num: 0 <= n <= 11

Read offset address: 510h + (Channel_num * 20h)

In Scatter/Gather DMA mode, various domains of this register is defined as follows:

Field	Note	Reset value	Access characteristics
31	Do ping(DoPng) It's only valid to OUT transmission, and when the bit is set to 1, it indicates the Host does the PING protocol. If the bit is set to 1 in IN transmission, this channel will be invalid	1'b0	R_W
30:29	PID(Pid) ●2'b00:DATA0 ●2'b01:DATA2 ●2'b10:DATA1 ●2'b11: MDATA (non-control)	2'b0	R_W
28:16	Reserved domain	9'b0	RO
15:8	NTD (the number of transmitting descriptors) (Non-real time transmission) ●0-1 descriptors ●63-64 descriptors (Real-time transmission) ●7-8 descriptors ●15-16 descriptors ●31-32 descriptors ●63-64 descriptors ●127-128 descriptors ●255-256 descriptors	8'h0	R_W
7:0	SCHED_INFO (scheduling information) The corresponding bit represents the angle in the microFrame. Bit0 represents the scheduling in 1st microFrame Bits7 represents the scheduling in 8th microFrame 8'b11111111 represents the scheduling of the corresponding interrupt channel and one token is sent every other microFrame in corresponding frame time. 8'b10101010 represents the scheduling of the corresponding interrupt channel and one token is sent every other microFrame in corresponding frame time. Note, this domain is only valid for periodic	8'h0	R_W

	transmission.		

In Non-Scatter/Gather DMA mode, various domains of this register are defined as follows:

Field	Note	Reset value	Access characteristics
31	Do ping(DoPng) It's only valid to OUT transmission, and when the bit is set to 1, it indicates the Host does the PING protocol. If the bit is set to 1 in IN transmission, this channel will be invalid	1'b0	R_W
30:29	PID(Pid) ●2'b00:DATA0 ●2'b01:DATA2 ●2'b10:DATA1 ●2'b11: MDATA (non-control)	2'b0	R_W
28:19	Packet number (PktCnt). Packet data of software write-in transmission. When one transmission finishes, host will reduce the domain by 1. Once it's 0, the software will receive the interrupt and indicate the normal end.	10'h0	R_W
18:0	Transmission size (XferSize) For OUT transmission, it specifies the number of bytes transited by host; for IN transmission, it specifies the number data bytes received by host.	19'h0	R_W

Host Channel-n DMA address register (HCDMAn)

Channel_num: 0 <= n <= 11

Read offset address: 514h + (Channel_num * 20h)

In IN/OUT transmission, the register is used to maintain the address of the current buffer. The starting address of DMA transmission must be double-word aligned.

<table>
<tr><th>Field</th><th>Note</th><th>Reset value</th><th>Access characteristics</th></tr>
<tr><td colspan="4">Buffer DMA Mode</td></tr>
<tr><td>31:0</td><td>DMA address (DMAAddr)
Transaction-post accumulation of each AHB</td><td>X</td><td>R_W</td></tr>
<tr><td colspan="4">Descriptor DMA mode</td></tr>
<tr><td>31: N (Real-time)
31:9 (Non-real time)</td><td>DMA address (DMAAddr)
Non-real time transmission: save the starting address of 512-byte page The first descriptor in descriptor list is in this address. OTG controller starts to process descriptor list from CTD
Real-time transmission: save the address of 2*(nTD+1) bytes, and the address is the location of the real-time descriptor. The N value is based on nTD, as shown in the table below:
<table>
<tr><td>31:N</td><td>N-1: 3</td><td>2:0</td></tr>
<tr><td>Base address</td><td>Offset</td><td>000</td></tr>
</table>
<table>
<tr><td>nTD</td><td>N</td></tr>
<tr><td>7</td><td>6</td></tr>
<tr><td>15</td><td>7</td></tr>
<tr><td>31</td><td>8</td></tr>
<tr><td>63</td><td>9</td></tr>
<tr><td>127</td><td>10</td></tr>
<tr><td>255</td><td>11</td></tr>
</table></td><td>23'h0</td><td>R/W</td></tr>
</table>

N-1: 3 (Real-time) 8: (Non-real time)	Current transmission descriptor (CTD) Non-real time transmission: its unit is descriptor and the range is 0-63. It indicates the current processing descriptor. Real-time transmission: based on the value of the current micorFrame, it needs clearing by software.	6'h0	R/W
2:0	Reserved	3'h0	RO

Host Channel-n DMA Buffer address register (HCDMAn)
Channel_num: 0 <= n <= 11
Read offset address: 518h + (Channel_num * 20h)
This is only valid in Scatter/Gather DMA mode

Field	Note	Reset value	Access characteristics
31:0	Current buffer address.	X	RO

Host Frame List base address register (HFLBAddr)
Offset: 41Ch
This is only valid in Scatter/Gather DMA mode

Field	Note	Reset value	Access characteristics
31:0	Initial address of frame list	32'h0	RO

13.3.4 Device Mode Register

This register block is only effective in device mode, and can't be accessed in host mode.

Device configuration register (DCFG)
Offset: 800h
After the initial configuration, the value of this register can't be modified.

Field	Note	Reset value	Access characteristics
31:26	Resume validity (ResValid) This domain controls the switch time of OTG controller from suspended state to resume. Clock period as a unit. Only when DCFG.Ena32KHzSusp is set to 1, this bit is significant.	6'd2	R_W
25:24	Periodic schedule interval (PerSchIntvl) Valid only in Scatter/Gather DMA mode. It's used to specify the time allocated by DMA engine to periodic IN endpoint to obtain data. Based on the number of periodic IN endpoints, its value must be set to 75%microFrame. ●When any periodic endpoint activates, DMA engine allocates certain time for periodic IN endpoint to obtain data. ●Ignore this domain when there is no periodic end node activity ●After the time is set, DMA engine begins to obtain data for non-periodic endpoint. ●2'b00: 25% microFrame ●2'b01: 50% microFrame ●2'b10: 75% microFrame ●2'b11: Reserved	2'b00	R_W
23	In device mode, Scatter/Gather DMA mode (DescDMA) is	1'b0	R_W

	enabled. ●GAHBCFG. DMAEn=0, DCFG. DescDMA=0 => from mode ●GAHBCFG. DMAEn=0, DCFG. DescDMA=1 => illegal ●GAHBCFG. DMAEn=1, DCFG. DescDMA=0 => buffer DMA mode ●GAHBCFG.DMAEn=0,DCFG.DescDMA=0=> Scatter/Gather DMA mode		
22:14	Reserved		RO
13	Whether to enable device OUT NAK Only valid for descriptor DMA mode ●1'b0: When the bulk OUT transfer ends, OTG controller doesn't send out the NAK handshaking signal. ●1'b0: When the bulk OUT transfer ends, OTG controller sends out the NAK handshaking signal.	1'b0	R_W
12:11	Periodic frame interval (PerFrInt) It indicates when one microFrame uses EOP interrupt to notify the software. This domain is used to decide whether the current microFrame has finished all real-time transfers. ●2'b00: 80% ●2'b01: 85% ●2'b00: 90% ●2'b00: 95%	2'h0	R_W
10:4	Device address (DevAddr)	7'h0	R_W
3	Reserved	1'b0	RO
2	Non-zero length Status OUT handshake (NZStsOUTHShk) If OTG receives a non-zero data packet in OUT event in the Status stage of control transfer, this domain is used to select different handshaking signals controlled and transmitted by OTG. ●1'b1: STALL ●1'b0: send out the received OUT data packet, and then transmit the handshaking signal based on NAK and STALL bits in device endpoint control register.	1'b0	R_W
1:0	Device speed (DevSpd) ●2'b00: HS(USB2.0 PHY) ●2'b01: FS(USB2.0 PHY) ●2'b10: LS(USB1.1 PHY) ●2'b11: FS(USB1.1 PHY)	2'b0	R_W

Device control register (DCTL)
Offset: 808h

Field	Note	Reset value	Access characteristics
31:17	Reserved		RO
16	Send out NAK handshake in the case of babble	1'b0	R_W
15	For real-time endpoint, ignore frame number (IgnrFrmNum) ●GAHBCFG. DMAEn=0, this domain is invalid ●GAHBCFG. DMAEn=1, DCFG. DescDMA = 0: When the threshold mode is valid, this bit is invalid. Or, the software uses this bit to enable the periodic transfer interrupt. -1'b0 invalid periodic transmission interruption - When 1'b1receives ISOC IN token, it doesn't need to clear the packet. OTG controller ignores the frame number, when the packet is prepared and receives the corresponding token, this packet will be sent out. This domain is also used to enable	1'b0	R_W

	periodic interrupt transmission • GAHBCFG. DMAEn=1, DCFG. DescDMA = 1: Invalid high-speed transmission		
14:13	Global Multi Count (GMC) Valid only in Scatter/Gater DMA mode. It is used to indicate the number of received and transmitted packets before transferred to next endpoint. Valid only for aperiodic end nodes. ●2'b00: Illegal ●2'b01: One package; ●2'b00: Two packages; ●2'b00: Three packages; When DCFG.DescDMA =1, this domain will be automatically changed to 2'h1	2'h0	R_W
12	Reserved domain		RO
11	Powr-on programming is done (PWROnPrgDone) After recovering from power_down mode, when the register programming is finished, the bit is set to 1.	1'b0	R_W
10	Clear Global OUT NAK (CGOUTNak) For the write to this bit, Clear Global OUT NAK	1'b0	WO
9	Set Global OUT NAK(SGOUTNak) For the write to this bit, set Global OUT NAK	1'b0	WO
8	Clear Global Non-periodic IN NAK (CGNPInNak) For the write to this bit, clear Global Non-periodic IN NAK	1'b0	WO
7	Set Global Non-periodic IN NAK (SGNPInNak) For the write to this bit, set Global Non-periodic IN NAK	1'b0	WO
6: 4	Test control (TstCtl) ●3'b000: Invalid Test mode ●3'b001: Test_J mode ●3'b010: Test_K mode ●3'b011: Test_SE0_NAK mode ●3'b100: Test_Packet mode ●3'b101: Test_Force_Enable mode ● Others: Reserved	3'b0	R_W
3	Global OUT NAK status (GOUTNakSts) ●1'b0: Based on FIFO status, NAK and STALL bit setup, corresponding handshake is transmitted. ●1'b1: No matter whether RxFIFO has the null term, no data is written in RxFIFO. Except SETUP event, all packets send NAK handshake. Termination of all real-OUT packet.	1'b0	RO
2	Global non-periodic IN NAK Status Bit ●1'b0: Based on valid data of TxFIFO, corresponding handshake is sent. ●1'b1: For all non-periodic IN endpoints, NAK handshake signals are transmitted, no matter whether TxFIFO has effective data.	1'b0	RO
1	Soft disconnection (SftDisCon) If this bit is set to 1, the host can't see device connection, and the device can't receive the USB signal. ●1'b0: Normal operation ●1'b1: OTG controller will set the phy_opmode_o signal in utmi+ interface to 2'b01, which will generate a disconnect event to the USB host.	1'b0	R_W
0	Remote Wakeup signal (RmtWkUpSig) When the bit is set to 1, the OTG controller will send a remote wakeup signal to wake up the USB host.	1'b0	R_W

Device status register (DSTS)
Offset: 808h

Field	Note	Reset value	Access characteristics
[31:22]	Reserved		RO
21:8	Received SOF Frame Number (SOFN)	14'h0	RO
7: 4	Reserved		RO
3	Serious error (ErrticErr) Through this domain, the OTG controller reports serious error (because PHY goes wrong, phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i setting exceeds 2ms). In the event of serious errors, the OTG controller will enter into the suspend mode, and GINTSTS.ErlySusp bit is set to 1, and only the software can recover through soft break.		RO
2:1	Enumeration speed (EnumSpd) ●2'b00: HS(USB2.0 PHY) ●2'b01: FS(USB2.0 PHY) ●2'b10: LS(USB1.1 PHY) ●2'b11: FS(USB1.1 PHY)		RO
0	Suspending status (SuspSts) In Device mode, as long as the suspend status found in USB bus, set it to 1. When utmi_linestate signal doesn't activate within certain event, the OTG controller will enter into the suspended state. The OTG controller will exit from the suspended state if —: ● utmi_linestate signal activates ●The software writes 1 in DCTL.RmtWkUpSig bit.	1'b0	RO

Device In Endpoint Common Interrupt Mask Register (DIEPMSK)
Offset: 810h

Field	Note	Reset value	Access characteristics
31:14	Reserved		RO
13	NAK Interrupt Mask Bit (NAKMsk)	1'h0	R_W
12:10	Reserved		RO
9	BNA Interrupt Mask Bit (BNAInIntrMsk) Valid only when descriptor is in the DMA mode	1'h0	R_W
8	FIFO Underflow Interrupt Mask Bit (TxFifoUndrnMSK)	1'b0	R_W
7	Reserved	1'b0	RO
6	IN endpoint NAK valid interrupt mask bit (INEPNakEffMsk)	1'b0	R_W
5	Receive the IN token interrupt mask bit mismatching EP (INTknEPMisMsk)	1'b0	R_W
4	When TxFIFO is empty and receives IN token interrupt mask bit (INTknTXFEmpMsk)	1'b0	R_W
3	Timeout interrupt mask bit (TImeOUTMsk) Valid only for non-real-time end node	1'b0	R_W
2	AHB error interrupt mask bit (AHBErrMsk)	1'b0	R_W
1	End nodes failure interrupt mask bit (EPDisbldMsk)	1'b0	R_W

0	Transmission completion interrupt mask bit (XferCompIMsk)	1'b0	R_W

device Out Endpoint Common Interrupt Mask Register (DIEPMSK)

◆ Offset: 814h

Field	Note	Reset value	Access characteristics
31:15	Reserved		RO
14	NYET interrupt mask bit (NYETMsk)	1'b0	R_W
12	Bubble interrupt mask bit (BbleErrMsk)	1'b0	R_W
11:10	Reserved		RO
9	BNA interrupt mask bit (BnaOutIntrMsk)	1'b0	R_W
8	OUT packet error interrupt mask bit (OutPktErrMsk)	1'b0	R_W
7	Reserved		RO
6	Receives the back-to-back SETUP packet interrupt mask bit (Back2BackSETup)	1'b0	R_W
5	Reserved		RO
4	When the endpoint is invalid and receives OUT token interrupt mask bit (OUTTknEPdisMsk)	1'b0	R_W
3	SETUP phase completion interrupt mask bit (SetUPMsk)	1'b0	R_W
2	AHB error interrupt mask bit (AHBErrMsk)	1'b0	R_W
1	End nodes failure interrupt mask bit (EPDisbldMsk)	1'b0	R_W
0	Transmission completion interrupt mask bit (XferComplMsk)	1'b0	R_W

Device all endpoints common interrupt register (DAINT)

◆ Offset: 818h

Field	Note	Reset value	Access characteristics
31:16	OUT endpoint interrupt register bit (OutEPInt) 1 OUT end node corresponding to 1 bit Bit 16 corresponding to the end node 0	16'h0	RO
15:0	IN endpoint interrupt register bit (InEPInt) 1 IN end node corresponding to 1 bit Bit 0 corresponding to the end node 0	16'h0	RO

Device all endpoints common interrupt register (DAINTMSK)

Offset:81Ch

Field	Note	Reset value	Access characteristics
31:16	OUT endpoint interrupt register bit (OutEPIntMsk) 1 OUT end node corresponding to 1 bit Bit 16	16'h0	R_W

	corresponding to the end node 0		
15:0	IN endpoint interrupt register bit (InEPIntMsk) 1 IN end node corresponding to 1 bit Bit 0 corresponding to the end node 0	16'h0	R_W

Device VBUS Discharge Register (DVBUSDIS)

Offset: 828h

Field	Note	Reset value	Access characteristics
31:16	Reserved		RO
15:0	Device Vbus Discharge Time (DVBUSDis) During SRP, the discharge time of Vbus after Vbus impulse. In PHY clock bit units.	30MHZ: 16'h0B8F 60MHZ: 16'h17D7	R_W

Device VBUS Pulse Register (DVBUSPULSE)

Offset: 82Ch

Field	Note	Reset value	Access characteristics
31:12	Reserved		RO
11:0	Device Vbus Pulse Time () During SRP, the pulse time of Vbus. In PHY clock bit units.	30MHZ: 12'h2c6 60MHZ: 12'h5b8	R_W

Device threshold value control register (DTHRCTL)

Offset: 830h

Field	Note	Reset value	Access characteristics
31:28	Reserved		RO
27	Arbiter parking enable	1'b1	R_W
26	Reserved		RO
25:17	Receive threshold length (RxThrLen)	9'h8	R_W
16	Receive threshold enable (RxTHrEn)	1'b0	R_W
15:13	Reserved		RO
12:11	AHB threshold ratio (AHBThrRatio)	2'b0	R_W
10:2	Transmit threshold length (TxThrLen)	9'h8	R_W
1	Real-time IN Endpoint Threshold Value Enable (ISOThrEn)	1'b0	R_W
0	Non-real Time IN Endpoint Threshold Value Enable (NonISOThrEn)	1'b0	R_W

Device IN Endpoint FIFO Empty Interrupt Mask Register (DIEPEMPMSK)

Offset: 834h

Field	Note	Reset value	Access characteristics
31:16	Reserved		RO
15:0	IN Endpoint Tx FIFO Empty Interrupt Mask Register (InEpTxfEmpMsk) As the interrupt mask bit of DIEPINTn, one bit corresponds to one endpoint.	16'b0	R_W

	Bit0 corresponds to endpoint 0, and so on.		

Device Control IN Endpoint 0 Control Register (DIEPCTL0)

Offset: 900h

Field	Note	Reset value	Access characteristics
31	End node enable (EPEna) ● In Scatter/Gather DMA mode, in terms of IN Endpoint, this threshold 1 means that the descriptor and data buffer have been prepared. ● In non- Scatter/Gather DMA mode, this threshold 1 means that the data buffer has been prepared. When OTG sets up the following interrupts, this bit will be cleared 0. ● End node failure ● Transmission completion	1'b0	R_WS_SC
30	End node failure (EPDis) The software sets the bit to 1, and will stop transmitting data to this endpoint even if the transfer isn't finished. The software must wait that the endpoint valid interrupt happens, can it think the endpoint has been invalid. When the OTG controller sets endpoint valid interrupt, clear the bit to 0, and only when EPEna bit is 1, set the bit to 1. This domain is valid only in DMA mode.	1'b0	R_WS_SC
29:28	Reserved		RO
27	Set NAk (SNAK) Set 1, set the NAK bit corresponding to this endpoint to 1.	1'b0	WO
26	Clear NAK (CNAK) Set 1, set the NAK bit corresponding to this endpoint to 0.	1'b0	WO
25:22	TxFIFO number (TxFNum) Set the FIFO number corresponding to IN endpoint 0.	4'h0	R_W
21	STALL handshake (Stall) When receiving SETUP packet, the software sets 1, and OTG controller clears 0. If NAK bit, global non-periodic IN NAK and Global OUT NAK bit are all set to 1, the priority of STALL bit will be the highest.	1'b0	R_WS_SC
20	Reserved		RO
19:18	Endpoint type (EPType) For the control node 2'b00	2'h0	RO
17	NAK status (NAKSts) ●1'b0: Based on FIFO status, OTG controller sends out Non-NAK handshake. ●1'b1: OTG controller transmission NAK handshake	1'b0	RO
16	Reserved		RO
15	USB Active Endpoint (USBActEP) If it has been 1, it means that the control endpoint 0 is always available.	1'b1	RO
14:2	Reserved		RO
1:0	The maximum packet size (MPS) ●2'b00: 64B ●2'b01: 32B ●2'b10: 16B ●2'b11: 8B	2'h0	R_W

Device Control OUT Endpoint 0 Control Register (DIEPCTL0)

Offset: B00h

Field	Note	Reset value	Access characteristics
31	End node enable (EPEna) ● In Scatter/Gather DMA mode, in terms of OUT Endpoint, this threshold 1 means that the descriptor and data buffer have been prepared to receive data. ● In non- Scatter/Gather DMA mode, this threshold 1 means that the data buffer has been prepared. When OTG sets up the following interrupts, this bit will be cleared 0. ● SETUP time phase completion ● End node failure ● Transmission completion In DMA mode, if OTG controller transfers SETUP data packet, the bit must be set to 1.	1'b0	R_WS_SC
30	End node failure (EPDis) The software can't invalidate OUT control node 0.	1'b0	RO
29:28	Reserved		RO
27	Set NAk (SNAK) Set 1, set the NAK bit corresponding to this endpoint to 1.	1'b0	WO
26	Clear NAK (CNAK) Set 1, clear the NAK bit corresponding to this endpoint to 1.	1'b0	WO
25:22	Reserved		RO
21	STALL handshake When receiving SETUP packet, the software sets 1, and OTG controller clears 0. If NAK bit, global non-periodic IN NAK and Global OUT NAK bit are all set to 1, the priority of STALL bit will be the highest. No matter whether this bit is set to 1, the handshake signal that OTG controller corresponds to SETUP data packet is always ACK.	1'b0	R_WS_SC
20	Snoop mode (Snp) In snoop mode, when transferring the data to the memory, the OTG controller doesn't check the correctness of OUT data packet.	1'b0	R_W
19:18	Endpoint type (EPType) For the control node 2'b00	2'h0	RO
17	NAK status (NAKSts) ●1'b0: Based on FIFO status, OTG controller sends out Non-NAK handshake. ●1'b1: OTG controller transmission NAK handshake	1'b0	RO
16	Reserved		RO
15	USB Active Endpoint (USBActEP) If it has been 1, it means that the control endpoint 0 is always available.	1'b1	RO
14:2	Reserved		RO
1:0	The maximum packet size (MPS) ●2'b00: 64B ●2'b01: 32B ●2'b10: 16B ●2'b11: 8B	2'h0	R_W

Device endpoint-n control register (DIEPCTLn/DOEPCTLn)

◆Endpoint_num: 1 <= n <= 6

◆Offset for IN: 900h + (Endpoint_num*20h)

◆Offset for OUT: B00h + (Endpoint_num*20h)

Field	Note	Reset value	Access characteristics
31	End node enable (EPEna) Applied in IN / OUT terminal nodes. ● In Scatter/Gather DMA mode, for IN endpoint, this threshold 1 means that the descriptor and data buffer have been prepared; for OUT endpoint, the threshold 1 means that the descriptor and data buffer have been prepared to receive data. ● In Scatter/Gather DMA mode, for IN endpoint, this threshold 1 means that the data buffer have been prepared to send data; for IN endpoint, the threshold 1 means that the data buffer have been prepared to receive data. When OTG sets up the following interrupts, this bit will be cleared 0. ● SETUP time phase completion ● End node failure ● Transmission completion	1'b0	R_WS_SC
30	End node failure (EPDis) Applied in IN / OUT endpoint. The software sets the bit to 1, and will stop transmitting data to this endpoint even if the transfer isn't finished. The software must wait that the endpoint valid interrupt happens, can it think the endpoint has been invalid. When the OTG controller sets endpoint valid interrupt, clear the bit to 0, and only when EPEna bit is 1, set the bit to 1.	1'b0	R_WS_SC
29	Set DATA1 PID (SetD1PID) It's only valid for interrupt/bulk IN and OUT endpoint. 1 is written in this bit, DPID bit is set to DATA1. It's valid for both descriptor DMA and non-descriptor DMA mode.	1'b0	WO
28	Set DATA0 PID (SetD1PID) It's only valid for interrupt/bulk IN and OUT endpoint. 1 is written in this bit, DPID bit is set to DATA0. It's valid for both descriptor DMA and non-descriptor DMA mode.	1'b0	WO
27	Set NAk (SNAK) Applied in IN / OUT endpoint. Set 1, set the NAK bit corresponding to this endpoint to 1.	1'b0	WO
26	Clear NAK (CNAK) Applied in IN / OUT endpoint. Set 1, clear the NAK bit corresponding to this endpoint to 1.	1'b0	WO
25:22	TxFIFO number (TxFNum) Valid only for IN end nodes; Set the FIFO number corresponding to IN endpoint.	4'h0	R_W
21	STALL handshake It's only valid for non-control and non-real time IN/OUT endpoint. Through the setup of this bit, stall all tokens from the host. If the NAK bit, global non-periodic NAK and global OUT NAK bit are all set to 1, the priority of STALL bit is the highest. No matter whether this bit is set to 1, the handshake signal that OTG controller corresponds to SETUP data packet is always ACK. Valid only for control end nodes. When receiving SETUP packet, the software is set to 1, and the OTG controller is cleared 0. If the NAK bit, global non-periodic NAK and global OUT NAK	1'b0	R_W

	bit are all set to 1, the priority of STALL bit is the highest. No matter whether this bit is set to 1, the handshake signal that OTG controller corresponds to SETUP data packet is always ACK.		
20	Snoop mode (Snp) Valid only for OUT endpoint; In snoop mode, when transferring the data to the memory, the OTG controller doesn't check the correctness of OUT data packet.	1'b0	R_W
19:18	Endpoint type (EPType) ●2'b00: Control ●2'b01: Real time ●2'b10: Bulk ●2'b11: Interrupt	2'h0	R_W
17	NAK status (NAKSts) Apply to all IN/OUT endpoints. ●1'b0: Based on FIFO status, OTG controller sends out Non-NAK handshake. ●1'b1: OTG controller transmission NAK handshake	1'b0	RO
16	End node data PID (DPID) Apply to interrupt/bulk IN and OUT endpoint. Include the PID of data packet received or sent by this endpoint. After this endpoint activates, the software must set the PID of the first packet received or sent by this endpoint. Use the SetD0PID and SetD1PID domains of this register to set DATA0 or DATA1 PID ● 1'b0: DATA0 ● 1'b1: DATA1 Odd-even frames (EO_FrNum) In the non-descriptor DMA mode, apply to the real-time IN/OUT endpoint. It appoints the frame number used by this endpoint to send or receive the real-time data. It's set by the SetEvnFr and SetOddFr domains of this register. ● 1'b0: Even frames ● 1'b1: Odd frames In the descriptor DMA mode, this domain bit remains the domain.	1'b0	RO
15	USB active end nodes Applied in IN / OUT endpoints. It appoints in current configuration and interface, whether the endpoint activates.	1'b0	R_W_Sc
14:11	Reserved		RO
10:0	The maximum packet size (MPS) Applied in IN / OUT endpoints. Set the maximum packet size, in bytes	11'b0	R_W

Device endpoint-n interrupt register (DIEPCTLn / DOEPCTLn)

- Endpoint_num: 1 <= n <= 6
- Offset for IN: 908h + (Endpoint_num*20h)
- Offset for OUT: B08h + (Endpoint_num*20h)

Field	Note	Reset value	Access characteristics
31:15	Reserved		RO
14	NYET interrupt (NYETIntrpt)	1'b0	R_SS_WC
13	NAK interrupt (NAKIntrpt)	1'b0	R_SS_WC
12	Bubble error interrupt (BbleErrIntrpt)	1'b0	R_SS_WC
11	Packet drop status (PktDrpSts)	1'b0	R_SS_WC

10	Reserved		RO
9	BNA (the buffer can't be used) interrupt (BNAIntr)	1'b0	R_SS_WC
8	FIFO underflow (TxFifoUndrn)	1'b0	R_SS_WC
7	TxFIFO empty (TxFEmp)	1'b0	R_SS_WC
6	IN endpoint NAK effectiveness (PNakEff)	1'b0	R_SS_WC
5	Receive IN token interrupt mismatching EP (INTknEPMis)	1'b0	R_SS_WC
4	When TxFIFO is empty and receives IN token interrupt (INTknTXFEmp)	1'b0	R_SS_WC
3	Overtime interrupt (TImeOUT) Valid only for non-real-time end node	1'b0	R_SS_WC
2	AHB error interrupt (AHBErr)	1'b0	R_SS_WC
1	End nodes failure interrupt (EPDisbld)	1'b0	R_SS_WC
0	Transmission completion interrupt (XferCompI)	1'b0	R_SS_WC

Device endpoint 0 transfer size register (DIEPTSIZ0/DOEPTSIZ0)

◆Offset for IN: 910h

◆Offset for OUT: B10h

For IN end nodes:

Field	Note	Reset value	Access characteristics
31:15	Reserved		RO
20:19	The number of packets (PktCnt) Indicate the number of packets in the number of transmission size. When reading a packet from TxFIFO, this domain decreases 1.	2'b0	R_W
18:7	Reserved domain	7'h0	R_W
6:0	Transmission size It indicates the transfer size of endpoint 0 (in the unit of byte), and when it exceeds this value, it will cause interrupt. It can be set MPS of this end node. Every time one packet is written in TxFIFO, this domain decreases 1.	7'h0	R_W

For OUT end nodes:

Field	Note	Reset value	Access characteristics
31	Reserved		RO
30:29	Number of SETUP packets (SUPPktCnt) It indicates the number of back-to-back SETUP packet received by this endpoint. ●2'b01: One package ●2'b10: Two packages; ●2'b11: Three packages;	2'b0	R_W
28:20	Reserved domain	7'h0	R_W
19	The number of packets (PktCnt) Every time one packet is written into RxFIFO, this domain decreases to 0.	1'b0	R_W
18:7	Reserved		RO
6:0	Transmission size (XferSize)	7'h0	R_W

	It indicates the transfer size of endpoint 0 (in the unit of byte), and when it exceeds this value, it will cause interrupt. It can be set MPS of this end node. When reading a packet from RxFIFO, this domain decreases 1.		

Device endpoint-n transfer size register (DIEPSIZn /DOEPSIZn)

◆Endpoint_num: 1 <= n <= 6
◆Offset for IN: 910h + (Endpoint_num*20h)
◆Offset for OUT: B10h + (Endpoint_num*20h)

Field	Note	Reset value	Access characteristics
31:29	Reserved		RO
30:29	MC (MultiCount) Valid only for IN end nodes. For the periodic IN endpoint, this domain indicates the number of packets transferred within one microFrame time. OTG controller uses this domain as the real-time IN endpoint to calculate the data PID. ●2'b01: One package; ●2'b10: Two packages; ●2'b11: Three packages; For non-periodic IN endpoint, it indicates OTG controller must be the number of packets obtained by this endpoint, when transferred to the next endpoint appointed by DIEPCTLn.Nextep. RxPID (received data PID) is only valid for the real-time OUT endpoint, the data PID of the last packet received by this endpoint. ●2'b00: DATA0 ●2'b01: DATA2 ●2'b10: DATA1; ●2'b11: MDATA; SETUP packets (SUPCnt) It's only valid for controlling OUT endpoint, indicating the number of back-to-back SETUP packets received by this endpoint. ●2'b01: One package ●2'b10: Two packages; ●2'b11: Three packages;	2'b0	R_W
28:19	The number of packets (PktCnt) It indicates the packet count under this transfer size (PktCnt = XferSize/MPS) ●IN endpoint: when one packet is read in TxFIFO, this domain reduces 1. ●OUT endpoint: when one packet is written in RxFIFO, this domain reduces 1.	10'h0	R_W
18:0	Transmission size (XferSize) Indicate the transfer size of the endpoint (in the unit of byte) ●When reading a packet from RxFIFO, this domain decreases 1. ● Every time one packet is written in TxFIFO, this domain decreases 1.	19'b0	R_W

Device endpoint-n DMA address register (DIEPDMAn/DOEPDMAn)

◆Endpoint_num: 1 <= n <= 6
◆Offset for IN: 914h + (Endpoint_num*20h)

◆Offset for OUT: B14h + (Endpoint_num*20h)

Field	Note	Reset value	Access characteristics
31:0	DMA address (DMAAddr) Save the initial address of external storage allocated to this endpoint. ● In non- Scatter/Gather DMA mode, it's the initial address. ● In Scatter/Gather DMA mode, it's the base address of the descriptor table	X	R_W

Device endpoint-n DMA Buffer Address Register (DIEPDMABn/DOEPDMABn)

◆Endpoint_num: 1 <= n <= 6
◆Offset for IN: 91Ch + (Endpoint_num*20h)
◆Offset for OUT: B1Ch + (Endpoint_num*20h)

Field	Note	Reset value	Access characteristics
31:0	DMA Buffer Address (DMABufferAddr) Save current buffer address. When the data is transferring in this endpoint, the address will be updated in real time. Valid only in Scatter/Gather DMA mode.	X	RO

Device IN Endpoint- nTxFIFO status register (DTXSTSn)

◆Endpoint_num: 1 <= n <= 6
◆Offset918h + (Endpoint_num*20h)

Field	Note	Reset value	Access characteristics
31:16	Reserved		RO
[15:0]	IN endpoint TxFIFO space available (INEPTxFSpcAvail) 32 bytes as unit. ●16'h0: End node TxFIFO full ●16'h1: One word available 。。。 ●16'hn: N words available ●Others: Reserved		RO

13.3.5 Power consumption and clock gating register

Power consumption and gating of clock control register （PCGCCTL）

◆OffsetE00h

Field	Note	Reset value	Access characteristics
31:9	Reserved		RO
8	Reset after suspended (ResetAfterSusp) If the host needs to reset after suspended, the soft needs to set this bit to 1 before clearing the clamp. If this bit isn't set to 1, the host will send out the reset signal after suspended.	1'b1	R_W
7	Deep sleep (L1 Suspended) In L1 status, PHY enters into the deep sleep	1'b0	RO
6	PHY sleep (PhySleep)	1'b0	RO

	PHY into sleep status.		
5	Enable the sleep gating (Enbl_L1Gating) If the OTG controller can't set the bit to utmi_l1_suspend_n, after the bit setup, the gating can't apply to the internal clock in deep sleep	1'b0	R_W
4	Reserved		RO
3	Reset power-down module (RstPdwnModule) In power-off, the software sets 1, and after power-on and PHY clock recovers, the software clear 0.	1'b0	R_W
2	Power supply isolation (PwrClmp) Before power off, the software sets the bit to 1 to isolate the power-on and power-off modules. Clear software to zero before power on	1'b0	R_W
1	Gating Hclk (GateHclk) It sets 1, when the USB in suspended state, use gating clock to Hclk. When the USB recovers or the new dialogue starts, the software clears 0.	1'b0	R_W
0	Stop Pclk (StopPclk) When the bit is set to 1, if the USB is under the suspended state, stop PHY clock. When the USB recovers or the new dialogue starts, the software clears 0.	1'b0	R_W

14 General Purpose DMA

Loongson 1C processor includes a DMA module, and has three ways of DMA, which is used to operate block data or stream data and enhance the working efficiency of processor. One IC chip has five modules (SDIO, ADC, AC97, I2S, NAND), and will use the general DMA. Three ways of DMA are configured by software.

14.1 DMA Controller Structural Description

The process of DMA transferring data consists of three stages:
1. The pretreatment before transfer: the CPU finishes the following steps: configure the registers related to DMA descriptor.
2. Data transfer: it is finished automatically under the control of DMA controller.
3. Transmission completion process: transmit an interrupt request.
The DMA controller is limited to the data transfer in the unit of byte (4 bytes). It designs the next descriptor address register, source address register, destination address register, transfer data counter, transfer step-length interval, transfer cycle index, DMA control logic, and other essential registers. The cache size of DMA is 128Byte (32x4Byte) and is read in the unit of byte.
Through the configuration of DMA register, CUP saves the data from memory or equipment in cache memory, and writes the data in buffer in the corresponding internal memory or equipment, and finally sends DMA end of transmission signal. During the DMA transfer, the CPU can monitor the working condition of DMA at any time.

14.2 DMA Register

14.2.1ORDER_ADDR_IN

English name: this register is broadcast to the three-way DMA, and the selected DMA starts the work on the bit width of register based on the register configuration. [31:0]
Address: 0xbfd0_1160
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:6	Ask_addr	26	R/W	The high 26 bits and low 6 bits of first descriptor address of the selected DMA are 0; equivalently, the Ask_addr of 26 bits left shifts 6 bits.
5	Reserved	1		
4	dma_stop	1	R/W	User request to stop the DMA operation; Stop operation after the completion of current data reading and writing operations
3	dma_start	1	R/W	It can start to read the first DMA descriptor of descriptor chain; When the register related to the first descriptor is red back, this bit is reset.
2	Ask_valid	1	R/W	The user requests to write relevant information of current DMA operation to the specified memory address. After the user writes backs relevant information of DMA operation, this bit is cleared.
1:0	Dev_num	2	R	2’b00 nand flash 2’b01 AC97 read device 2’b10 AC97 write device

Note:

The address of the first descriptor is in ORDER_ADDR_IN register, and the register is configured by CPU, namely, Ask_addr lef shifts 6 bits and composes the base address of the descriptor register.
In each DMA operation, the address and significant bit of the next descriptor saved by DMA_ORDER_ADDR register. If ask_valid=1, it indicates the CPU will monitor the DMA operation, and the value of DMA controller register is written back to the memory directed by ask_addr.
If dma_start=1, it indicates the DMA operation starts. The DMA reads the descriptor from the memory address directed by ask_addr, and starts to implement DMA operation based on descriptor information.

14.2.2DMA_ORDER_ADDR

English name: next descriptor address register
Register bit width: [31:0]
Base address: reset if the descriptor address is five bits lower.
Offset address: 0x0
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:1	dma_order_addr	31	R/W	Next descriptor address register of internal memory
0	Dma_order_en	1	R/W	If descriptor is a valid signal

Notes: to store the address of the next DMA descriptor, dma_order_en is the enable bit of the next DMA descriptor. If the bit is 1, it indicates the descriptor is valid, and if the bit is 0, it indicates the descriptor is invalid. Don't perform operation, and the address of 16 bytes is aligned. In the configuration of DMA descriptor, the register stores the address of the next descriptor, and after the DMA operation is performed, determine whether to start the next DMA operation by judging dma_order_en signal.

14.2.3DMA_SADDR

English name: memory address register
Register bit width: [31:0]
Base address: reset if the descriptor address is five bits lower.
Offset address: 0x4
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:0	dma_saddr	32	R/W	DMA operation memory address

Notes: the DMA operation is divided as follows: read the data from memory, and save them in the buffer of DMA controller; the APB sends the request to access the data in DMA buffer, and the register specifies the address of read memory; read the data from APB device, and save them in DMA buffer. When the number of words in DMA buffer exceeds certain amount, the data will be written in memory, and the register has specified the address of write memory

14.2.4 DMA_DADDR

English name: device address register
Register bit width: [31:0]
Base address: reset if the descriptor address is five bits lower.
Offset address: 0x8
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31		1	R/W	AC97 write enables, "1" indicates the write operation.
30		1	R/W	0: mono 1: 2 stero
29:28		2	R/W	AC97 write mode, 0: 1byte, 1: 2byte, 2: 4 byte

27:0	dma_daddr	32	R/W	APB device address in DMA operation

Notes: read the data from memory and save them in the buffer of DMA controller; the APB sends the request to access the data in DMA buffer, and the register specifies the address of read memory; read the data from APB device, and save them in DMA buffer. When the number of words in DMA buffer exceeds certain amount, the data will be written in memory, and the register has specified the address of read APB device.

14.2.5 DMA_LENGTH

English name: length register
Register bit width: [31:0]
Base address: reset if the descriptor address is five bits lower.
Offset address: 0xc
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:0	dma_length	32	R/W	Transmission data length register

Notes: it represents the length of one block of transported content, and its unit is byte. After the length word is transported, the next step starts, namely, next cycle. A new cycle starts, and the length word is transported again. When the step becomes 1, the single DMA descriptor operation ends, and it starts to read the next descriptor.

14.2.6DMA_STEP_LENGTH

English name: interval length register
Register bit width: [31:0]
Base address: reset if the descriptor address is five bits lower.
Offset address: 0x10
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:0	dma_step_length	32	R/W	Data transmission interval length register

Notes: the interval lengths indicates the length between two transported memory data blocks, and the interval between the end address of the previous step and the start address of the next step.

14.2.7DMA_STEP_TIMES

English name: cycle index register
Register bit width: [31:0]
Base address: reset if the descriptor address is five bits lower.
Offset address: 0x14
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:0	dma_step_times	32	R/W	Data transmission cycle index register

Notes: the cycle time indicates the number of blocks to be transported in one DMA operation. If it intends to transport one continuous data block, the value of cycle time register is assigned 1.

14.2.8 DMA_CMD

English name: control register
Register bit width: [31:0]
Base address: reset if the descriptor address is five bits lower.
Offset address: 0x18
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
14:13	Dma_cmd	2	R/W	Generation types of source and destination address
12	dma_r_w	1	R/W	DMA operation type, "1" is read memory and write device, "0" is read device and write memory.
11:8	dma_write_state	4	R/W	DMA write data status
7:4	dma_read_state	4	R/W	DMA read data status
3	dma_trans_over	1	R/W	DMA implements the configured descriptor operations.
2	dma_single_trans_over	1	R/W	Complete the implementation of one DMA descriptor operation
1	dma_int	1	R/W	DMA interrupt signal
0	dma_int_mask	1	R/W	If DMA interrupts are masked out
Bit field	Bit field name	Bit width	Access	Description

Notes: dma_single_trans_over=1 indicates that one DMA operation implementation finishes, and length=0 and step_times=1, and it starts to pick up the descriptor of the next DMA operation. The descriptor address of the next DMA operation is saved in DMA_ORDER_ADDR register, and if in DMA_ORDER_ADDR register dma_order_en=0, dma_trans_over=1 and the entire dma operation finishes without new descriptor to read; if dma_order_en=1, dma_trans_over is set to 0, and it starts to read the next dma descriptor. dma_int is the DMA interrupt, and if without the interrupt mask, the interrupt occurs after one configured DMA operation finishes. After the CPU deals with interrupt, it's set to low directly. Equivalently, the DMA is automatically set low in next transfer. dma_int_mask is the interrupt mask corresponding to dma_int. dma_read_state indicates the current read state of DMA. dma_write_state indicates the current read state of DMA.

DMA write state (WRITE_STATE[3:0]) description, DMA includes the following write states:

Write_state	[3:0]	Description
Write_idle	4'h0	Idle writing status
W_ddr_wait	4'h1	Dma judgment needs to perform the operation of read device and write memory, and sends the memory request. But when the memory hasn't prepared the response request, dma has been waiting for the memory response.
Write_ddr	4'h2	The memory has received dma write request, but hasn't performed the write operation.
Write_ddr_end	4'h3	The memory receives dma write request, and finishes the write operation, and then the dma is in the state of finishing the operation of write memory.
Write_dma_wait	4'h4	Dma sends out the request of dma status register writes back to memory, and waits for the memory to receive request.
Write_dma	4'h5	The memory receives the request of write dma status, but the operation hasn't finished.
Write_dma_end	4'h6	Memory completing writing dma status operation
Write_step_end	4'h7	Dma finishes one length operation (namely, one step)

DMA write state (WRITE_STATE[3:0]) description, DMA includes the following read states:

Read_state	[3:0]	Description
Read_idle	4'h0	Idle read status
Read_ready	4'h1	Receive the start signal of starting dma operation, enters into the read state, and starts to read descriptors.
Get_order	4'h2	It sends the request of reading descriptor to the memory, and waits for the response of memory.

Read_order	4'h3	The memory receives the request of reading descriptor, and is performing the read operation.
Finish_order_end	4'h4	Memory completing reading dma descriptor
R_ddr_wait	4'h5	Dma sends the request of reading data to the memory, and waits for the response of memory.
Read_ddr	4'h6	The memory receives the request of dma read data, and is performing the read operation.
Read_ddr_end	4'h7	The memory finishes the one request of read data of dma
Read_dev	4'h8	Dma into the reading device status
Read_dev_end	4'h9	The device returns the read data, and ends the request of reading the device.
Read_step_end	4'ha	After one step operation is finished, step times decrease 1.

14.3 Multiple Modules Use DMA Configuration Description

If some module needs to perform DMA operation, it needs to send the request to req signal of DMA. Through the configuration of misc_ctrl register, only after the req signal of this module is connected to req[2:0] signal of DMA, the DMA can be used normally.

Therein, the priority of SDIO is the highest, and can be configured to any way among three channels; when SDIO doesn't use the 0 channle, NAND uses 0 channel; when SDIO doesn't use the 1st channel, I2S and AC97 multiplex the 1st channel; when SDIO doesn't use the 2nd channel, ADC, 2S and AC97 multiplex the 2nd channel. ADC priority is higher than I2S and AC97

DMA multiplexes the configuration corresponding to misc_ctrl[25:22]. Therein, misc_ctrl[22] is adc_dma_en, misc_ctrl[24:23]is sdio_dma_en, misc_ctrl[25]为 ac97_en.

For example, SDIO uses the 1st channel, ADC the 2nd channel, NAND the 0 channle, it should be configured as follows:

sdio_dma_en is 2, adc_dma_en is 1, ac97 and I2S can't use DMA.

For example, SDIO uses the Channel 0, ADC the 2nd channel, I2S the 1st channel, it should be configured as follows:

sdio_dma_en is 1, adc_dma_en is 1, ac97_en is 0.

15 SPI0 Controller

Serial peripheral equipment interface SPI bus technology is a full duplex, synchronous and serial data interface standard between several types of microprocessors, microcontrollers and peripheral equipment launched by Motorola company.

15.1 SPI Controller Architecture

The SPI controller integrated can only act as the host and connect slave. In terms of the software, except several IO registers, SPI controller has one section mapped to the read-only memory space of SPI Flash. If this section of memory space is allocated in 0xbfc00000, after reset it can be accessed directly without software intervention, so as to support processor startup from SPI Flash. The base address of IO register of SPI is 0xbfe8_0000, and the external storage address space is 0xbd00_0000 -0xbd7f_ffff, 8MB in total.

Its architecture is shown in Figure 15-1, and consists of AXI internal bus interface, simple SPI master controller, SPI Flash read engine, and bus selection modules. Based on access address and type, the legal request from internal bus interface is forward to SPI master controller or SPI Flash read engine (the illegal request is abandoned).

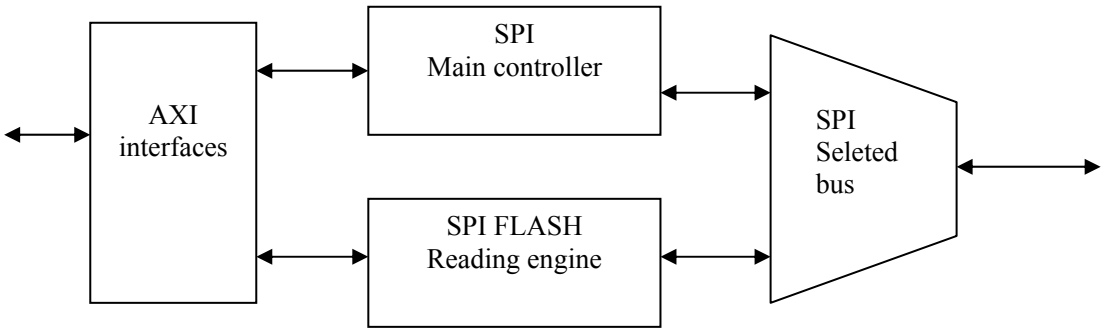

Figure 15-1 SPI controller architecture

15.2 Configuration Register

Offset	Name	Description
0	SPCR	Control register
1	SPSR	Status register
2	TxFIFO/RxFIFO	DR (data register)
3	SPER	Internal register
4	SFC_PARAM	Parameter control register
5	SFC_SOFTCS	Chip selection control register
6	SFC_TIMING	Sequence control register

15.2.1 Control register (SPCR)

Bit field	Name	Access	Initial value	Description
7	spie	R/W	0	Interrupt output enable signal active high
6	spe	R/W	0	System work enable signal active high
5	-	-	0	Reserved
4	mstr	-	1	Master mode selects the bit, and the bit remains at 1.
3	cpol	R/W	0	Clock polarity bit
2	cpha	R/W	0	If the clock phase bit is 1, the phase is opposite, and if it is 0, the phase is the same.

1:0	spr	R/W	0	sclk_o frequency division setup needs to be used with spre of sper together.

15.2.2 Status register (SPSR)

Bit field	Name	Access	Initial value	Description
7	spif	R/W	0	The interrupt flag bit 1 indicates that there is interrupt request, write 1 and reset.
6	wcol	R/W	0	When the write register overflow flag bit is 1, it indicates that it has overflowed, write 1 and reset.
5:4	-	-	0	Reserved
3	wffull	R	0	Write register full flag 1 indicating full
2	wfempty	R	1	Write register empty flag 1 indicating empty
1	rffull	R	0	Read register full flag 1 indicating full
0	rfempty	R	1	Read register empty flag 1 indicating empty

15.2.3 Data register (TxFIFO/RxFIFO)

Bit field	Name	Access	Initial value	Description
7:0	TxFIFO RxFIFO	W R	-	Data transmission port Data receiving port

15.2.4 External register (SPER)

Bit field	Name	Access	Initial value	Description
7:6	icnt	R/W	0	Transmit interrupt after several bytes transmission 00: 1 01: 2 10: 3 11: 4
5:3	-	-	-	Reserved
2	mode	R/W	0	spi interface mode control 0: Sample simultaneous with the transmission opportunity 1: Stagger half period of sampling and transmission opportunity
1:0	spre	R/W	0	Set fractional frequency ratio with spr

Table 15-1 SPI frequency division factor

spre spr	00 00	00 01	00 10	00 11	01 00	01 01	01 10	01 11	10 00	10 01	10 10	10 11
Frequency coefficient	2	4	16	32	8	64	128	256	512	1024	2048	4096

15.2.5 Parameter control register (SFC_PARAM)

Bit field	Name	Access	Initial value	Description
7:4	clk_div	R/W	2	Clock frequency selection

				Frequency division factor and {spre, spr} combination are the same.
3	dual_io	R/W	0	Dual I/O mode, the priority is higher than quick read.
2	fast_read	R/W	0	Quick reading mode
1	burst_en	R/W	0	SPI flash supports the continuous address read mode
0	memory_en	R/W	1	SPI flash read enables, if invalid, csn[0] can be controlled by software.

Notes: when programmed to SPI flash via EJTAG, it needs to set memory_en to 0.

15.2.6 Chip selection control register (SFC_SOFTCS)

Bit field	Name	Access	Initial value	Description
7:4	csn	R/W	0	csn pin-out output value
3:0	csen	R/W	0	When the bit is 1, the csn line corresponding to the bit is controlled by 7:4 bit

15.2.7 Timing sequence control register (SFC_TIMING)

Bit field	Name	Access	Initial value	Description
7:3	-	-	-	Reserved
2	tFAST	R/W	0	SPI flash read sampling mode 0: Along the sampling, interval of half SPI period 1: Along the sampling, interval of one SPI period
1:0	tCSH	R/W	3	The shortest invalid time of the chip selection signal of SPI Flash is calculated by the clock cycle T after frequency division 00: 1T 01: 2T 10: 4T 11: 8T

15.3 Interface Time Sequence

15.3.1 Timing sequence of SPI Master controller interface

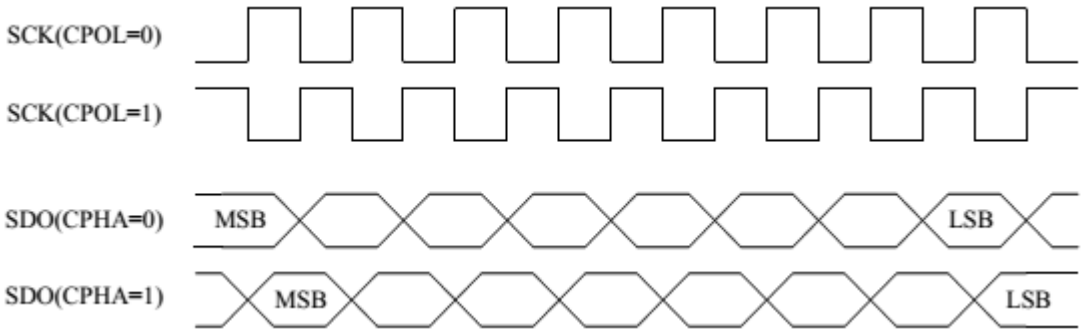

Figure 15-2 Timing sequence of SPI Master controller interface

15.3.2 SPI Flash access timing sequence

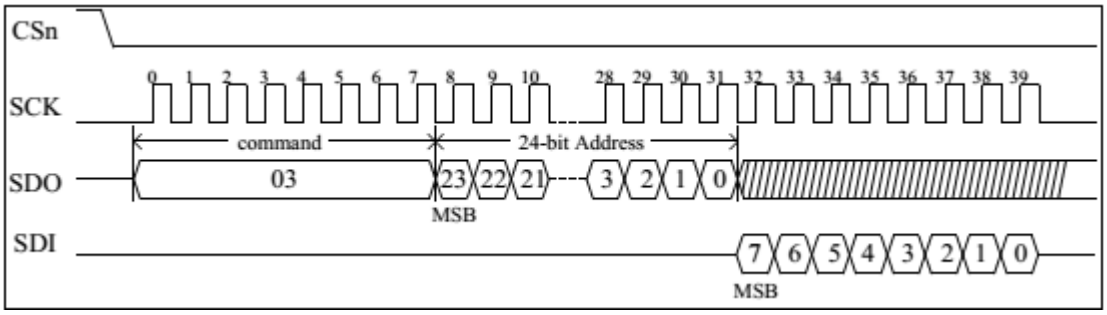

Figure 15-3 SPI Flash standard read timing sequence

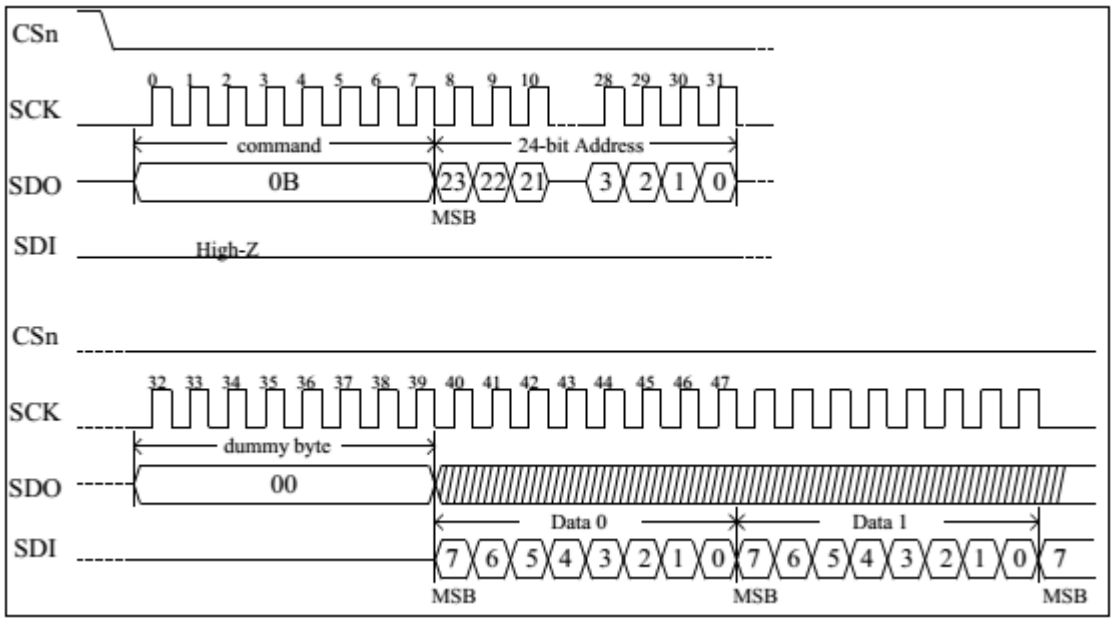

Figure 15-4 SPI Flash rapid read timing sequence

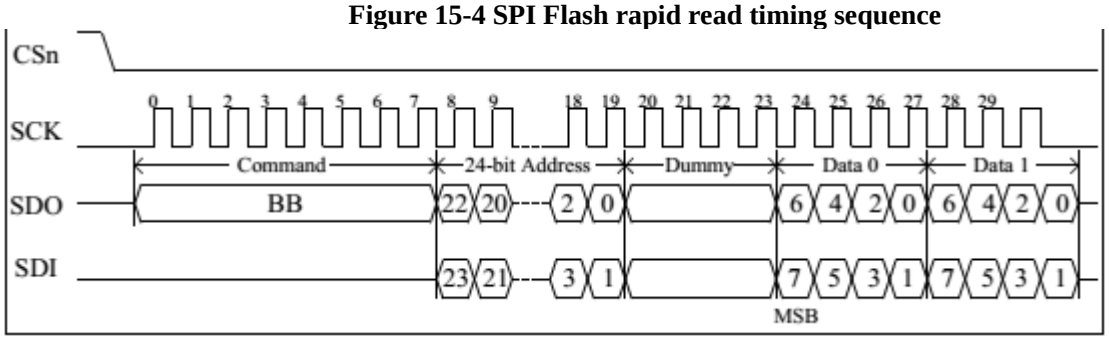

Figure 15-5 SPI Flash directional I/O read timing sequence

15.4 User's Manual

15.4.1 Read and write operations of SPI master controller

1. Module initialization

- Stop SPI controller work, write 0 to the spe bit of control register spcr
- Reset state register spsr, write 8'b1100_0000 to register
- Set the external register sper, including the condition for interrupt request sper[7:6] and frequency division factor sper[1:0]. Refer to register introduction.
- The configuration of SPI timing sequence includes the cpol and cpha of spcr, and mode bit of sper. When the mode is 1, it's the standard SPI implementation, and when the mode is 0, it's the compatible mode.
- Configuration interrupt enable, the spie bit of spcr

● Start SPI controller, and write 1 to spe bit of control register spcr

2. Module transmission / transfer operations

● Write data in the data transmission register

● After the transmission finishes, read the data from the data transfer register. Because the transmission and receipt happen simultaneously, even if SPI hasn't sent effective data from the equipment, the read operation must be performed.

3. Interrupt processing

●Receive the interrupt request

● Read the data of status register spsr, if spsr[2] is 1, it indicates the data transmission has finished, and if spsr[0] is 1, it indicates it has received the data.

●Read or write data transmission register

●Write 1 to spif bit of status register spsr, and clear the interrupt request of the controller

15.4.2 Hardware SPI flash head

1. Initialization

● Write 1 to the memory_en bit of SFC_PARAM. When the SPI is choosen as the starting device, this bit is reset to 1.

● Set read parameters (clock frequency division, continuous address read, quick read, dual I/O, tCSH, etc.) These parameter reset values are the most conservative.

2. Change the parameters

If the used SPI Flash supports higher frequency or provides the enhancement, the access speed of Flash can be quickened greatly by modifying corresponding parameters. The parameter modification doesn't need to close SPI Flash read enable (memory_en)). Specific reference register instructions.

15.4.3 Mixed access to SPI Flash and SPI master controller

●Access SPI Flash except read

After SPI Flash read enable shuts down, the software can directly control csn[0], and access SPI bus via SPI master controller. It means that when performing this operation, instructins can't be fetched from SPI Flash.

Except read, SPI Flash has implemented many commands (for example, erasion and write in), please refer to relevant Flash files.

16 SPI1 Controller

Serial peripheral equipment interface SPI bus technology is a full duplex, synchronous and serial data interface standard between several types of microprocessors, microcontrollers and peripheral equipment launched by Motorola company.

16.1 SPI Master Controller Architecture

The implementation of SPI1 and SPI0 is the same, and the system start address won't be mapped to SPI1 controller, so SPI1 doesn't support system start. The base address of IO register of SPI1 is 0xbfec0000, and the external storage address space of SPI1 is 0xbe00,0000 -0xbe3f,ffff, 4MB in total. Please refer to Chapter 15 information for all architectures and configurations

17 AC97 Controller

17.1 Overview (1C2 does not have this module)

One AC97 application system in system is as shown in Figure 19-1. In one system on chip, three parts are connected with AC97 controller: frstly, the peripheral bus to receive the control information and configuration from microprocessor; secondly, AC97 Codec, multimedia digital signal coder decode that modulates PCM signal, outputs the analogue voice received by human ears or convert the real sound to PCM singal; the conversion is implemented via D/A convertor; thirdly, DMA engine, DMA is configured by microprocessor, and transports the data from the memory area set by processor to FIFO or transports the data from FIFO to the set memory area.

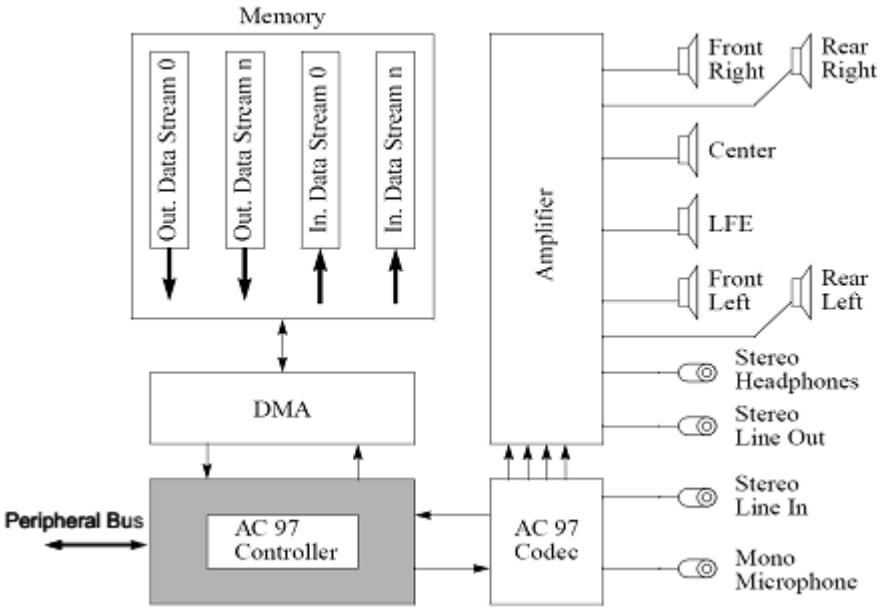

Figure 17-1 AC 97 application system

17.2 AC97 Controller Register

The base address of the physical address of this module register is 0xbfe6_0000.

Register name	Width	Offset	Description
CSR	2	0x00	Configuration status register
OCC0	24	0x04	Output channel configuration register 0
OCC1	24	0x08	Reserved
OCC2	24	0x0C	Reserved
ICC	24	0x10	Input channel configuration register
CODEC_ID	32	0x14	Codec ID register
CRAC	32	0x18	Codec register access command
OC0	20	0x02	Output sound track 0
OC1	20	0x24	Output sound track 1
OC2	20	0x28	Reserved
OC3	20	0x2c	Reserved
OC4	20	0x30	Reserved
OC5	20	0x34	Reserved
OC6	20	0x38	Reserved

OC7	20	0x3c	Reserved
OC8	20	0x40	Reserved
IC0	20	0x44	Reserved
IC1	20	0x48	Reserved
IC2	20	0x4c	Input sound track 2
INTRAW	32	0x54	Interrupt status register
INTM	32	0x58	Interrupt mask
INTS	32	0x5c	Reserved

17.2.1 CSR register

English name: configuration status register
Register bit width: [31:0]
Offset: 0x00
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:2	Reserved	30	RO	Reserved
1	RESUME	1	R/W	Get suspended, read this bit and returns to the state of the current AC97 subsystem. 1: AC97 suspend subsystem 0: normal working In the suspended state, write 1 to this bit, and start the recovery operation.
0	RST_FORCE	1	W	AC97 cold start Write 1, and cause the cold start of AC97 Codec

17.2.2 OCC register

English name: output channel configuration register
Register bit width: [31:0]
Offset: 0x04
Reset value: 0x00004141

Bit field	Bit field name	Bit width	Access	Description
31:24	Reserved	8	R/W	Reserved
23:16	Reserved	8	R/W	Reserved
15:8	OC1_CFG_R	8	R/W	Output channel 1: right sound track configuration
7:0	OC0_CFG_L	8	R/W	Output channel 0: left sound track configuration

17.2.3 ICC register

English name: input channel configuration register
Register bit width: [31:0]
Offset: 0x10
Reset value: 0x00410000

Bit field	Bit field name	Bit width	Access	Description
31:24	Reserved	8	R/W	Reserved
23:16	IC_CFG_MIC	8	R/W	Input channel 2: MIC channel configuration.
15:8	Reserved	8	R/W	Reserved

7:0	Reserved	8	R/W	Reserved

The configuration format of sound channels in OCC and ICC registers are the same, namely, OC0_CFG_L and OC0_CFG_R domains in OCC register and IC_CFG_MIC domain of OCC register in 17.2.3, and the format of sound track is shown as follows:

Bit field	Bit field name	Bit width	Access	Description
7	Reserved	1	R/W	Reserved
6	DMA_EN	1	R/W	DMA Enable 1: DMA Open 0: DMA Close
5:4	FIFO_THRES	2	R/W	FIFO threshold 5:4 Output channels input channels 00: FIFO 1/4 empty FIFO 1/4 full 01: FIFO 1/2 empty FIFO 1/2 full 10: FIFO 3/4 empty FIFO 3/4 full 11: FIFO fully empty FIFO fully full
3:2	SW	2	R/W	Sampling resolution 00:8 bit 10:16 Bit
1	VSR	1	R/W	Sampling rate 1: Variable sampling rate 0: Fixed sampling rate (48KHz)
0	CH_EN	1	R/W	Channel enable 1: Channel open 0: Channel shutdown (or enter a power-saving status)

17.2.4 Codec register access command

English name: Codec register access command
Register bit width: [31:0]
Offset: 0x18
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31	CODEC_WR	1	R/W	Read / Write selection 1: read, when reading the data, set CODEC_WR to read, and set the register address to be accessed in CODEC_ADR; after returning to data complete interrupt, reread value from CODEC_DAT register. 0: Write
30:23	Reserved	8	R	Reserved
22:16	CODEC_ADR	7	R/W	Codec register address
15:0	CODEC_DAT	16	R/W	Codec register data

17.2.5 Interrupt status register/interrupt mask register

English name: interrupt status / interrupt mask register
Register bit width: [31:0]
Offset: 0x54/58
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description

31	IC_FULL	1	R/W	Input channel 2: FIFO full
30	IC_TH_INT	1	R/W	Input channel 2: FIFO threshold reached
29:8	Reserved	22	R/W	Reserved
7	OC1_FULL	1	R/W	Output channel 1: FIFO full
6	OC1_EMPTY	1	R/W	Output channel 1: FIFO empty
5	OC1_ TH_INT	1	R/W	Output channel 1: FIFO threshold reached
4	OC0_FULL	1	R/W	Output channel 0: FIFO full
3	OC0_EMPTY	1	R/W	Output channel 0: FIFO empty
2	OC0_ TH_INT	1	R/W	Output channel 0: FIFO threshold reached
1	CW_DONE	1	R/W	Codec register writing is completed
0	CR_DONE	1	R/W	Codec register read is completed

17.2.6 Interrupt status / clear register

English name: interrupt status / clear register
Register bit width: [31:0]
Offset: 0x 5c
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:0	INT_CLR	32	RO	The masked interrupt status register, the read operation of this register will clear all interrupt states in register 0x54

17.2.7 OC Interrupt clear register

English name: OC interrupt clear
Register bit width: [31:0]
Offset: 0x60
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:0	INT_OC_CLR	32	RO	The read operation of this register will clear bit[7:2] corresponding to all output channel interrupt states in register 0x54

17.2.8 IC Interrupt clear register

English name: IC interrupt clear
Register bit width: [31:0]
Offset: 0x64
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:0	INT_IC_CLR	32	RO	The read operation of this register will clear bit[31:30] corresponding to all output channel interrupt states in register 0x54

17.2.9 CODEC WRITE interrupt clear register

English name: CODEC WRITE interrupt clear
Register bit width: [31:0]
Offset: 0x68
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description

31:0	INT_CW_CLR	32	RO	The read operation in this register will clear the bit[1] in register 0x54

17.2.10 CODEC READ interrupt clear register

English name: CODEC READ interrupt clear
Register bit width: [31:0]
Offset: 0x 6c
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
31:0	INT_CR_CLR	32	RO	The read operation in this register will clear the bit[0] in register 0x54

18 I2C Controller

18.1 Overview

This chapter has provided the details, configuration and use of I2C The chip in system integrates I2C interfaces, and is mainly used to implement the data exchange between two devices. I2C bus is the serial bus consistuted by data line SDA and clock SCL, and can send and receive data. The bidirectional transfer is conducted between devices, Loongson 1C has integrated three-way I2C interfaces in total.

18.2 I2C Controller Architecture

Main modules of I2C master controller architecture include Clock Generator, Byte Command Controller, Bit Command controller, and Data Shift Register. The rest are LPB bus interfaces and some registers.
Clock generator module: generate the frequency division clock, sync bit command. Byte command controller module: interpret one command to the timing sequence of operation by bytes, namely, the byte operation is decomposed into bit operation.
Bit command controller module: conduct the transmission of actual data, and the generation of bit command signal.
Data shift register module: serial data shift

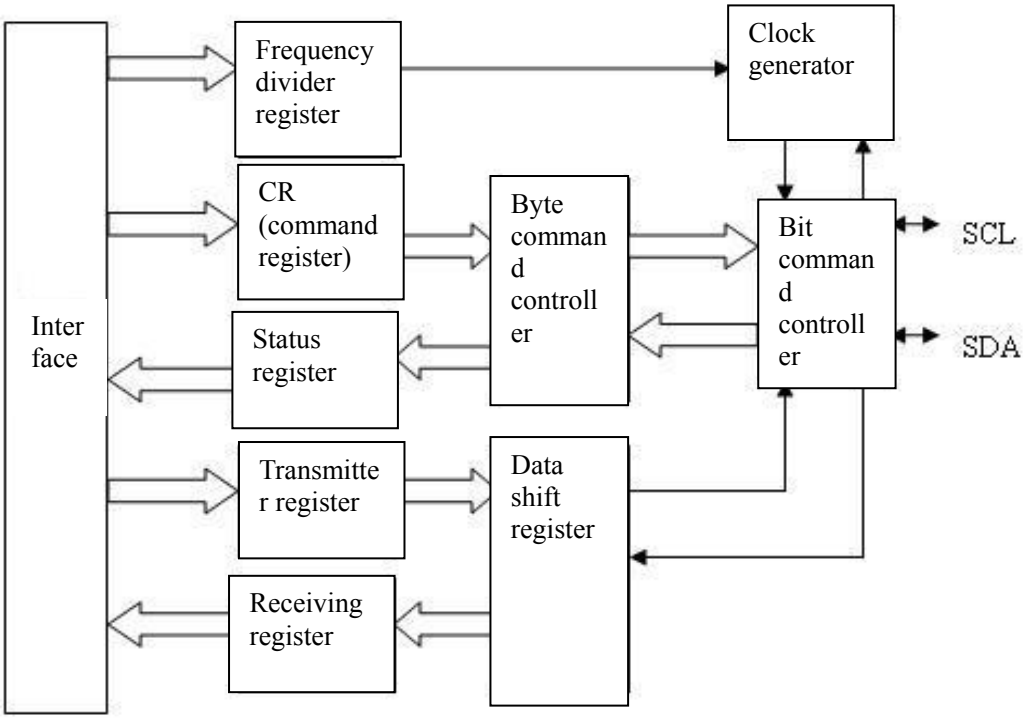

Figure 18-1 I2C Master Controller architecture

18.3 I2C Controller Register Description

The base address of the physical address of I2C-0 module register is 0xbfe5_8000, and the address space is 16KB.
The base address of the physical address of I2C-1 module register is 0xbfe6_8000, and the address space is 16KB.
The base address of the physical address of I2C-2 module register is 0xbfe7_0000, and the address space is 16KB.

18.3.1 Frequency division latch low-byte register (PRERlo)

English name: frequency division latch low-byte register register bit width: [7:0]
Offset: 0x00
Reset value: 0xff

Bit field	Bit field name	Bit width	Access	Description
7:0	PRERlo	8	RW	Fractional frequency latch storage low 8

18.3.2 Frequency division latch high-byte register (PRERhi)

English name: Fractional frequency latch high byte register
Register bit width: [7:0]
Offset: 0x01
Reset value: 0xff

Bit field	Bit field name	Bit width	Access	Description
7:0	PRERhi	8	RW	Fractional frequency latch storage high 8

The frequency of frequency division clock clock_a in module is half of DDR_clk frequency (see Chapter 29 for DDR_clk configuration); assuming that the value of frequency division latch is prescale, the output frequency of SCL bus is clock_s (the clock is determined based on user's demand and external I2C equipment characteristics), and should meet the following conditions:

Prcescale=clock_a/(5*clock_s)-1
Or Prcescale=DDR_clk/(10*clock_s)-1

18.3.3 Control register (CTR)

English name: control register
Register bit width: [7:0]
Offset: 0x02
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	EN	1	RW	When the module wrok enable bit is 1, it's the normal operating pattern, and when it's 0, the frequency division register can operate.
6	IEN	1	RW	If interrupt enable bit is 1, open the interrupt
5:0	Reserved	6	RW	Reserved

18.3.4 Transmit data register (TXR)

English name: transmit register
Register bit width: [7:0]
Offset: 0x03
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7:1	DATA	7	W	Store next byte to be transmitted
0	DRW	1	W	In data transfer, this bit saves the lowest bit of the data; in address transfer, this bit indicates read and write statuses

18.3.5 Receive data register (RXR)

English name: Receiving register

Register bit width: [7:0]
Offset: 0x03
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7:0	RXR	8	R	Store the last received byte

18.3.6 Command control register (CR)

English name: Command register
Register bit width: [7:0]
Offset: 0x04
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	STA	1	W	Generate START signal
6	STO	1	W	Generate STOP signal
5	RD	1	W	Generate read signal
4	WR	1	W	Generate write signal
3	ACK	1	W	Generate acknowledge signal
2:1	Reserved	2	W	Reserved
0	IACK	1	W	Generate interrupt acknowledge signal

The hardware is automatically cleared after the I2C sends data. In bit read operartions, it's always read back to '0'.

18.3.7 Status register (SR)

English name: Status register
Register bit width: [7:0]
Offset: 0x04
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	RxACK	1	R	Receive acknowledge bit 1 fail to receive acknowledge bit 0 receive acknowledge bit
6	Busy	1	R	I 2c Bus busy flag bit 1 busy bus 0 idle bus
5	AL	1	R	When I2C core loses I2C bus control right, this bit is set to 1.
4:2	Reserved	3	R	Reserved
1	TIP	1	R	Indicate transmission process 1 indicate data is being transmitted 0 indicate data transmission is completed
0	IF	1	R	Interrupt flag bit, when one data transfer is finished or another device initiates the data transfer, this bit is set to 1.

19 UART Controller

19.1 Overview

IC integrates 12 UART controllers, and communicates via APB bus and bus bridge. UART controller provides the function of serial communication with MODEM or other external equipment, for example, communicate with another computer by serial links according to the standard of RS232. The controller design is well compatible with international industrial standard semi-conductor equipment 16550A.
UART controller supports the expansion to USART mode by configuration register. The USART controller complies with two basic protocols: T=0 and T=1 in ISO7816, and provides the support for infrared and smart card interface modes.

19.2 Controller Architecture

The UART controller has Transmitter and Receiver modules, MODEM module, Interrupt Arbitrator module, and Register Access Control module, and their relationship is shown in the figure below. Main module functions and features are described below:

● Transmitter and receiver modules: be responsible for sending and receiving the data frame. The transmitter module converts the parallel data in FIFO transmit queue to serial data frame in the set form, and sends them through send port. The receiver module monitors the signal in receiving end, and in case of significant start bit, it will receive and convert the asyn serial data frame into parallel data, store them in FIFO receive queue, and check that the data frame format is right. The frame structure of UART is set by line control register (LCR), and the status of transmitter and receivers is stored in line control register (LCR).

● MODEM module: MODEM control register (MCR) controls the status of output signals DTR and RTS. MODEM control module monitoring the line status of input signals DCD, CTS, DSR and RI, and record the state of those signals in the bit corresponding to MODEM status register.

● Interrupt Arbitrator module: when any interrupt condition is met, and the corresponding bit of interrupt enable register is set to 1, the interrupt request signal UAT_INT of UART is set to significant condition. In order to reduce the interaction with external software, UART divides the interrupt into four grades, and identifies these interrupts in interrupt identification register (IIR). The interrupt at four levels rank as follow is in the order of priority: receive line status interrupt; receive data ready for interrupt; transfer the empty interrupt with register; MODEM status interrupt.

● Access to register module: when UART module is selected, CPU can access to the register selected by address line by read or write operations.

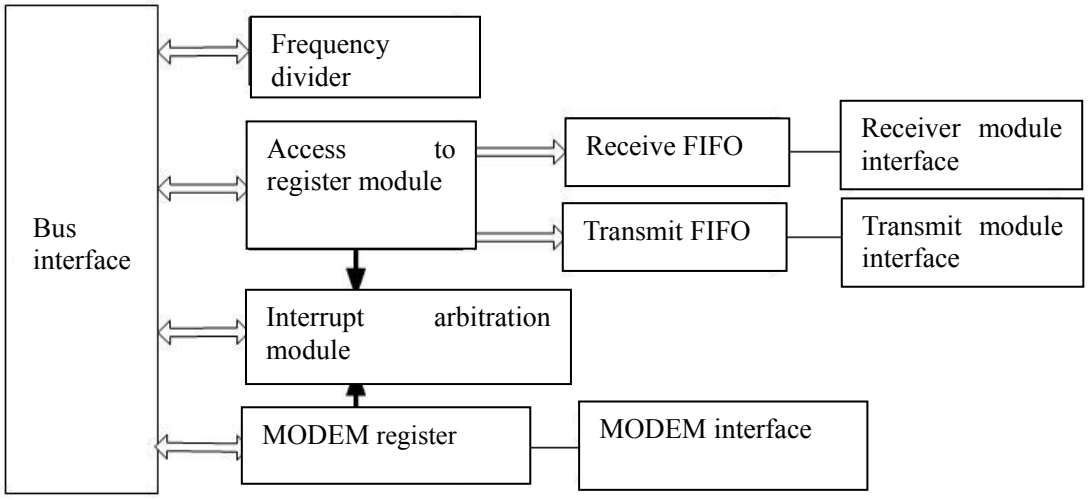

Figure 19-1 UART controller architecture

The expanded part of USART has added relevant register supporting ISO7816 specification, modified the receiver and transmitter modules, and added functions of receiving and transmitting error checking and retransmission control.

19.3 UART0 Split Configuration Introduction

Global fuction interfaces of UART0 in Loongson can be divided into two four-wire serial ports. See section 5.2.4 SHUT_CTRL[31:30] for configuration register.
When UART_split = 0, the pin of UART0 is the global function serial port of UART00.
When UART_split = 1, the UART0 is divided into two controllers: UART00 and UART01. The global functional pin of UART acts as four-wire serial output of two serial ports: UART00 and UART01, and their relationship is shown as follows:

Table 19-1 Configuration and function multiplexing of UART split

Original UART0 function pin-out	Uart_split= 0	Uart_split= 1
UART0_TXD	UART00_TXD	UART00_TXD
UART0_RTS	UART00_RTS	UART00_RTS
UART0_DTR	UART00_DTR	UART01_TXD
UART0_RI	UART00_RI	UART01_RTS
UART0_RXD	UART00_RXD	UART00_RXD
UART0_CTS	UART00_CTS	UART00_CTS
UART0_DSR	UART00_DSR	UART01_RXD
UART0_DCD	UART00_DCD	UART01_CTS

The function register of UART0 and UART01 is completely the same with the register described in 19.4, but the access base address is different. Therein, the base address of register physical address of UART00 is 0xbfe4_0000, and that of UART01 is 0xbfe4_1000.

19.4 Register Description

Loongson 1C has 12 UART/USART (marked as URT) interface, and its function is completely the same with functional register, but the access base address is different.

- The base address of register physical address of URT0 is 0xbfe4_0000.
- The base address of register physical address of URT1 is 0xbfe4_4000.
- The base address of register physical address of URT2 is 0xbfe4_8000.
- The base address of register physical address of URT3 is 0xbfe4_c000.
- The base address of register physical address of URT4 is 0xbfe4_c400.
- The base address of register physical address of URT5 is 0xbfe4_c500.
- The base address of register physical address of URT6 is 0xbfe4_c600.
- The base address of register physical address of URT7 is 0xbfe4_c700.
- The base address of register physical address of URT8 is 0xbfe4_c800.
- The base address of register physical address of URT9 is 0xbfe4_c900.
- The base address of register physical address of URT10 is 0xbfe4_ca00.
- The base address of register physical address of URT11 is 0xbfe4_cb00.

19.4.1 Data register (DAT)

English name: Data transmission register

Register bit width: [7:0]
Offset: 0x00
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7:0	Tx FIFO	8	W	Data transmitter register

19.4.2 Interrupt enable register (IER)

English name: Interrupt enable register
Register bit width: [7:0]
Offset: 0x01
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7:4	Reserved	4	RW	Reserved
3	IME	1	RW	Modem status interrupt enables '0' – off '1' -on
2	ILE	1	RW	Receiver line status interrupt enable '0' – off '1' -on
1	ITxE	1	RW	Transfer and storage register is empty interrupt enable '0' – off '1' -on
0	IRxE	1	RW	Receive valid data interrupt enable '0' – off '1' -on

19.4.3 Interrupt identification register (IIR)

English name: Interrupt source register
Register bit width: [7:0]
Offset: 0x02
Reset Value: 0xc1

Bit field	Bit field name	Bit width	Access	Description
7:4	Reserved	4	R	Reserved
3:1	II	3	R	Interrupt source indicating bit, details in the table below
0	INTp	1	R	Interrupt indicating bit

Interrupt control function table:

Bit 3	Bit 2	Bit 1	Priorities	Interrupt type	Interrupt source	Interrupt reset control
0	1	1	1st	Receive line status	Odd-even, overflow or framing error, or break interrupt	Reading LSR
0	1	0	2nd	Receive valid number	The character number of FIFO reaches the trigger level.	The character number of FIFO is lower than trigger value.
1	1	0	2nd	Receive timeout	There is at least one character in FIFO, but there is no any operation within the time of four characters, including read and write operations.	Reading reception FIFO
0	0	1	3rd	Transmit, save and storage Empty device	Empty transmission save register	Write data to THR or multiple IIR

0	0	0	4th	Modem status	CTS, DSR, RI or DCD.	Read MSR

19.4.4 FIFO control register (FCR)

English name: FIFO control register
Register bit width: [7:0]
Offset: 0x02
Reset value: 0xc0

Bit field	Bit field name	Bit width	Access	Description
7:6	TL	2	W	Receive the trigger value '00' -1 byte '01' -4 bytes '10' -8 bytes '11' -14 bytes from interrupt request of FIFO
5:3	Reserved	3	W	Reserved
2	Txset	1	W	'1' clears the content sent to FIFO, and reset its logic
1	Rxset	1	W	'1' clears the content received from FIFO, and reset its logic
0	Reserved	1	W	Reserved

19.4.5 Line control register (LCR)

English name: Line control register
Register bit width: [7:0]
Offset: 0x03
Reset value: 0x03

Bit field	Bit field name	Bit width	Access	Description
7	dlab	1	RW	Fractional frequency latch access bit '1 '- Access operation fractional frequency latch '0 '- Access operation normal register
6	bcb	1	RW	Interrupt control bit '1' –the serial output is set to 0 (interrupt status) '0'—normal operation
5	spb	1	RW	Specified parity check bit '0 '- No specified parity check bit '1' –if LCR[4] bit is 1, transfer and check the parity check bit is 0. If LCR[4] bit is 0, transfer and check the parity check bit is 1.
4	eps	1	RW	Parity check bit selection '0' –there is an odd number of 1 in each character (including data and parity check bit) 1 '- there are an even number of characters in each character
3	pe	1	RW	Parity check bit enable '0 '- No parity check bit '1' – generate the parity check bits in output, and judge the parity check bits in input.
2	sb	1	RW	Digits of defined generation stop bit '0 '- 1 stop bit '1' –in case of five-bit length, there is 1.5 stop bits, and other lengths are 2 stop bits.
1:0	bec	2	RW	Set the digits of each character '00' -5 bit '01' -6 bit '10' -7 bit '11' -8 bit

19.4.6 MODEM control register (MCR)

English name: Modem control register
Register bit width: [7:0]
Offset: 0x04
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7:5	Reserved	3	W	Reserved
4	Loop	1	W	Loopback mode control bit '0'—normal operation '1'—- loopback mode. In loopback mode, TXD output has been 1, and the output shift register is directly connected to input shift register. Other connections are as follows. DTR DSR RTS CTS Out1 RI Out2 DCD
3	OUT2	1	W	Connect to DCD input in the loopback mode
2	OUT1	1	W	Connect to RI input in the loopback mode
1	RTSC	1	W	RTS signal control bit
0	DTRC	1	W	DTR signal control bit

19.4.7 Line status register (LSR)

English name: Line status register
Register bit width: [7:0]
Offset: 0x05
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	ERROR	1	R	Error indicating bit '1' – at least one of parity check bit error, frame error or interrupt. '0 '- No error
6	TE	1	R	Empty transmission indicating bit '1' –transfer FIFO and transfer shift register are empty. Cleared when writing data to the FIFO transmission '0 '- with data
5	TFE	1	R	Transmit empty FIFO bit indicating bit '1' –the current transfer FIFO is empty, reset when writing data to transfer FIFO '0 '- with data
4	BI	1	R	Break interrupt indicating bit 1' –receive start bit + data + parity bit + stop bit are all 0, namely, there is interrupt '0 '- no interrupt
3	FE	1	R	Frame error indicating bit '1 '- No stop bit in the received data '0 '- No error
2	PE	1	R	Error bit of parity check bit '1 '- parity error in current receiving data '0 '- No parity error
1	OE:	1	R	Data overflow indicating bit

				'1 '- Data overflow '0 '- No overflow
0	DR	1	R	Indicating bit of valid received data

Bit field	Bit field name	Bit width	Access	Description
				'0 '- No data in the FIFO '1 '- with data in the FIFO

During the read operation of the register, LSR[4:1] and LSR[7] are cleared; when writing data to transfer FIFO, LSR[6:5] is cleared, and LSR[0] judges received FIFO.

19.4.8 MODEM status register (MSR)

English name: Modem status register
Register bit width: [7:0]
Offset: 0x06
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	CDCD	1	R	The opposite of DCD input value or connect Out2 in loopback mode
6	CRI	1	R	The opposite of RI input value or connect to Out1 in loopback mode
5	CDSR	1	R	The opposite of DSR input value or connect to DTR in loopback mode
4	CCTS	1	R	The opposite of CTS input value or connect to RTS in loopback mode
3	DDCD	1	R	DDCD indicating bit
2	TERI	1	R	RI edge detection. RI status changes from low to high
1	DDSR	1	R	DDSR Indication bit
0	DCTS	1	R	DCTS Indication bit

19.4.9 Fractional frequency latch

English name: Fractional frequency latch 1
Register bit width: [7:0]
Offset: 0x00
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7:0	LSB	8	RW	Fractional frequency latch storage low 8 bit

English name: Fractional frequency latch 2
Register bit width: [7:0]
Offset: 0x01
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7:0	MSB	8	RW	Fractional frequency latch storage high 8 bit

19.5 USART Register Description

On the basis of UART, USART adds registers CR, MR and FIDIR supporting ISO7816 specification.

19.5.1 Control register (CR)

English name: control register
Register bit width: [7:0]
Offset: 0x8
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
0	UART_EN	1	RW	Serial port enable 0: Disable 1: Enable
1	IRDA_EN	1	RW	Infrared interface enable 0: Disable 1: Enable
2	SC_EN	1	RW	Smart card interface enable 0: Disable 1: Enable
3-7	-	-	-	Reserved

19.5.2 Mode register (MR)

English name: Mode register
Register bit width: [7:0]
Offset: 0x9
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
0-3	USART_MODE	4	RW	USART working mode: 0000: Normal 0001: Serial 0010: Hardware handshake 0011: modem 0100: ISO7816 T=0 0110: ISO7816 T=1 1000: IrDA Others: reserved
4-7	-	-	-	Reserved

19.5.3 FI/DI parameter register (FIDIR)

English name: Mode register
Register bit width: [31:0]
Offset: 0xA
Reset value: 0x00000000

Bit field	Bit field name	Bit width	Access	Description
0-10	FI_DI_RATIO	11	RW	0: ISO7816 mode doesn't generate Baud rate signal 1~2047: ISO7816 produces Baud rate signal
11-31	-	-	-	Reserved

20 NAND Controller

20.1 NAND Controller Structural Description

NAND FLASH controller supports four chip selections and four RDY signals at most, and the controller supports the operation of two types of FLASH (SLC and MLC), supports 512Bytes, 2K, 4K, 8K page size FLASH operations, supports single chip of 8GB, 32GB for four chips. NAND FLASH controller supports the system startup, and the startup mode includes ECC mode startup and ordinary mode startup.
The system startup mode selection includes two types, as is shown in following table:

Startup mode	Configuration	Note
ECC mode Start	NAND_CLE external pull-up	The content of the first page in external NAND FLASH must be data produced by original data via RS (204,188) decoding.
Normal startup	NAND_CLE external pull-down	The first page data of the external NAND FLASH is ordinary original data.

20.2 NAND Control Register Configuration Description

The list of NAND internal registers is as follows:

Address	Register name
0xbfe7_8000	NAND_CMD
0xbfe7_8004	ADDR_C
0xbfe7_8008	ADDR_R
0xbfe7_800C	NAND_TIMING
0xbfe7_8010	ID_L
0xbfe7_8014	STATUS
0xbfe7_8018	NAND_PARAMETER
0xbfe7_801C	NAND_OP_NUM
0xbfe7_8020	CS_RDY_MAP
0xbfe7_8040	DMA

20.2.1 Command register (NAND_CMD)

Bit	Bit field name	RW (read/write)	Description
31	DMA_REQ	R/-	In non-ECC mode, NAND sends DMA request.
30	ECC_DMA_REQ	R/-	In ECC mode, NAND sends DMA request.
29:25	STATUS	R/-	Internal status machine (for testing)
24		R/-	Reserved
23: 20	NAND_CE	R/-	Selection of external NAND chips and four bits correspond to four chip selections respectively. 0 stands for being chosen.
19: 16	NAND_RDY	R/-	In case of RDY of external NAND chip, the corresponding relationship is consistent with NAND_CE, and 1 indicates ready.
15			Reserved
14	Wait_rs_rd_done	R/W	1 indicates waiting for ECC read to finish (used in ECC read)
13	INT_EN	R/W	NAND interrupt enable signal, and 1 indicates

			enable interrupt.
12	RS_WR	R/W	1 indicates that ECC function is started in read operation.
11	RS_RD	R/W	1 indicates that ECC function is started in read operation.
10	done	R/W	1 indicates that the operation is finished, and it needs the software to clear.
9	Spare	R/W	1 indicates the operation occurs in SPARE area of NAND.
8	Main	R/W	1 indicates the operation occurs in MAIN area of NAND.
7	Read status	R/W	1 indicates the status operation of read NAND.
6	Reset	R/W	1 indicating Nand reset operation
5	read id	R/W	1 indicating reading ID operations
4	blocks erase	R/W	Erase the flag continuously, and default 0; 1 is valid, and the number of continuous erasing blocks are decided by nand_op_num.
3	erase operation	R/W	1 indicating erasure operation
2	write operation	R/W	1 indicating write operation
1	read operation	R/W	1 indicating read operation
0	command valid	R/W	1 indicates the command is valid, and the hardware is automatically cleared after operation.

20.2.2 Page offset address register (ADDR_C)

Bit	Bit field name	RW (read/write)	Description
31:14		R/-	Reserved
13:0	Nand_Col	R/W	Read, write and erase the initial address of the page address operation (it must be aligned by words, multiples of 4), and its corresponding relation with page size is: 512Bytes: it only needs to fill out [8:0] 2K: it needs to fill out [11:0], and [12] represents spare area, and [11:0] represents page offset address. 4K: it needs to fill out [12:0], and [12] represents spare area, and [11:0] represents page offset address. 8K: it needs to fill out [13:0], and [12] represents spare area, and [11:0] represents page offset address.

20.2.3 Page address register (ADDR_R)

Bit	Bit field name	RW (read/write)	Description
31:25		R/-	Reserved
24:0	Nand_Row	R/W	Read, write and erase operations start address, page address, and the address consists of: {Chip selection, pages} The chip selection is fixed to 2 bits, and the page number is determined based on actual capacity of single particle. For example, 1M page is [19:0], and [21:20] is used select which chip among 4 chips.

20.2.4 Timing sequence register (NAND_TIMING)

Bit	Bit field name	RW (read/write)	Description
31:16		R/-	Reserved
15:8	Hold cycle	R/W	The cycle number required by NAND command significant, default 4
7:0	Wait cycle	R/W	Total clock cycle number required by NAND one-time read and write, default 18, and configure to 8'hb in ECC mode

20.2.5 ID register (ID_L)

Bit	Bit field name	RW (read/write)	Description
[31:0]	ID (310)	R/-	ID (310)

20.2.6 ID and status register (STATUS & ID_H)

Bit	Bit field name	Access	
31:24		R/-	Reserved
23:16	STATUS	R/-	Current reading and writing completion status of NAND device
15:0	ID (4732)	R/-	ID high 16 bits (if the ID has only 5 bytes, ID[47:40] is 0)

20.2.7 Parameter configuration register (NAND_PARAMETER)

Bit	Bit field name	RW (read/write)	Description
31:30		R/-	Reserved
29:16	op_scope	R/W	Each capable operating range, the configuration is as follows: 1. Operate main area, and configure it to the size of the main area in a page 2. Operate spare area, and configure it to the size of the spare area in a page 3. Operate the main and spare areas, and configure to the size of the main and spare areas in a page
15		R/-	Reserved
14:12	ID_number	R/W	The number of bytes of the ID
11:8	External grain capacity size	R/W	0:1 Gb (2K page) 1:2 Gb (2K page) 2:4 Gb (2K page) 3:8 Gb (2K page) 4:16 Gb (4K page) 5:32 Gb (8K page) 6:64 Gb (8K page) 7:128 Gb (8K page) 9:64 Mb (512B page) a: 128Mb (512B page) b: 256Mb (512B page) c: 512Mb (512B page)

			d: 1Gb (512B page)
7:0		R/-	Reserved

20.2.8 Operating number register (NAND_OP_NUM)

Bit	Bit field name	RW (read/write)	Description
31:0	NAND_OP_NUM	R/W	NAND read and write Byte numbers (must be aligned by words, and multiples of 4); erase block number

20.2.9 Map register (CS_RDY_MAP)

Four CSs of NAND are automatically generated by the accessed address hardware, and CS0/RDY0 corresponds to the lowest space, CS1/RDY1 to the next lowest space, and so forth. If it's necessary to adjust the relationship between external chip and NAND address, remap cs_rdy 1/2/3 by setting this register.

Bit	Bit field name	RW (read/write)	Description
31:28	rdy3_sel	R/W	rdy3 signal is mapped from chip pin to NAND controller 4'b0001:NAND_RDY[0] 4'b0010:NAND_RDY[1] 4'b0100:NAND_RDY[2] 4'b1000:NAND_RDY[3]
27:24	cs3_sel	R/W	rdy3 signal is mapped from NAND controller to chip pin 4'b0001:NAND_CS[0] 4'b0010:NAND_CS[1] 4'b0100:NAND_CS[2] 4'b1000:NAND_CS[3]
23:20	rdy2_sel	R/W	rdy2 signal is mapped from chip pin to NAND controller 4'b0001:NAND_RDY[0] 4'b0010:NAND_RDY[1] 4'b0100:NAND_RDY[2] 4'b1000:NAND_RDY[3]
19:16	cs2_sel	R/W	cs2 signal is mapped from NAND controller to chip pin 4'b0001:NAND_CS[0] 4'b0010:NAND_CS[1] 4'b0100:NAND_CS[2] 4'b1000:NAND_CS[3]
15:12	rdy1_sel	R/W	rdy1 signal is mapped from chip pin to NAND controller 4'b0001:NAND_RDY[0] 4'b0010:NAND_RDY[1] 4'b0100:NAND_RDY[2] 4'b1000:NAND_RDY[3]
11:8	cs1_sel	R/W	cs1 signal is mapped from NAND controller to chip pin 4'b0001:NAND_CS[0] 4'b0010:NAND_CS[1] 4'b0100:NAND_CS[2] 4'b1000:NAND_CS[3]
7:0		R/-	Reserved

20.2.10 DMA read and write data register (DMA_ADDRESS)

Bit	Bit field name	RW (read/write	Description

		)	
[31£º0]	DMA_ADDRESS	R/W	For the access address where DMA reads and writes NAND flash data (except ID/STATUS), the read/write address is the same and the read/write direction is implemented by DMA configuration.

20.3 NAND ADDR Description

Taking 2K-page NAND flash for example, it's defined as follows:
The size of the main area in each page is 2KB, and that of the spare area is 64B

main_op = NAND_CMD[8];

spare_op = NAND_CMD[9];

addr_in_page ={A11, A10.. A2, A1, A0}=ADDR_C page_number ={ …A30,A29,A28,A27…A13,A12}= ADDR_R
Total capacity of computational formula of main area NAND flash
Capacity=2^(ADDR_C-1) * 2^(ADDR_R)*8bit = 2K*2^(ADDR_R)*8bit
NAND address space is exampled in the following table:

Table 20-1 NAND address space diagram

	I/O	0	1	2	3	4	5	6	7
Column1	1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
Column2	2nd Cycle	A8	A9	A10	A11	L.	L.	L.	L.
Row1	3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
Row2	4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
Row3 (Note)	5th Cycle	A28	A29	A30	A31	A32	A33	….	….

(Notes: the maximum Row corresponding to 2K-page 1Gb NAND flash is A27, and only Column1~2 and Row1~2 are used instead of Row3 to the address to NAND flash. In the configuration of NAND parameters, attention should be paid to the model configuration, or data won't be read and the controller may die, etc.)
For NAND particles in system board, if only the spare area is operated, A11=1 will be the only sign. Thus, when the software configures the internal register, it's necessary to configure A11 and spare_op to 1 (see Examples5). See Examples2 for wrong examples.
For NAND particles in system panel, if only the spare area is operated, A11=1 is the only sign. Thus, when the software configures the internal register, it's necessary to configure A11 and spare_op to 0 (see Examples1). See Examples4 for wrong examples.
For NAND particles in system panel, if only main+spare areas are operated, A11 may be 0 (see Examples3), and may also be 1 (See Examples6)

Examples1: (In non-ECC mode, One-page data in NAND particles is only located in 0x0-0x83f. The first op indicates the initial read and write data, and the following ops indicate the subsequent read and write data; NO_op indicates the data that can't be read and written by this NAND configuration.
(spare_op = 1'b0 & main_op =1'b0) equal to (spare_op = 1'b0 & main_op=1'b1); ADDR_C =0x30

Data in a page	0	0x30	….	0x7ff	0x800	0x830	0x83f
Page 0	NO_op	op	op	op	NO_op	NO_op	NO_op
Page 1	op	op	op	op	NO_op	NO_op	NO_op
Page 2	op	op	op	op	NO_op	NO_op	NO_op

Examples2:
spare_op=1'b1 & main_op=1'b0; ADDR_C = 0x30 (Wrong configuration!! The initial operation isn't performed in spare area, and the figure below shows the possible sequence of wrong access)

Data in a page	0	0x30	….	0x7ff	0x800	0x830	0x83f
Page 0	NO_op	op	op	op	Op	op	op
Page 1	NO_op	NO_op	NO_op	NO_op	Op	op	op
Page 2	NO_op	NO_op	NO_op	NO_op	Op	op	op

Page 3	NO_op	NO_op	NO_op	NO_op	Op	op	op

Examples3:
spare_op = 1'b1 & main_op =1'b1; ADDR_C = 0x30

Data in a page	0	0x30	….	0x7ff	0x800	0x830	0x83f
Page 0	NO_op	op	op	op	op	op	op
Page 1	op	op	op	op	op	op	op
Page 2	op	op	op	op	op	op	op

Examples4:
(spare_op=1'b0 & main_op=1'b0), (equal to spare_op=1'b0 & main_op=1'b1); ADDR_C=0x830: Wrong configuration!! The initial operation is performed in spare area, and the figure below shows the possible sequence of wrong access)

Data in a page	0	0x30	….	0x7ff	0x800	0x830	0x83f
Page 0	NO_op	NO_op	NO_op	NO_op	NO_op	NO_op	NO_op
Page 1	NO_op	op	op	op	op	NO_op	NO_op
Page 2	op	op	op	op	op	NO_op	NO_op
Page 3	op	op	op	op	op	NO_op	NO_op

Examples5:
spare_op = 1'b1 and main_op =1'b0; ADDR_C = 0x830

Data in a page	0	0x30	….	0x7ff	0x800	0x830	0x83f
Page 0	NO_op	NO_op	NO_op	NO_op	NO_op	op	op
Page 1	NO_op	NO_op	NO_op	NO_op	op	op	op
Page 2	NO_op	NO_op	NO_op	NO_op	op	op	op

Examples6:
spare_op = 1'b1 & main_op =1'b1; ADDR_C = 0x830

Data in a page	0	0x30	….	0x7ff	0x800	0x830	0x83f
Page 0	NO_op	NO_op	NO_op	NO_op	NO_op	op	op
Page 1	op	op	op	op	op	op	op
Page 2	op	op	op	op	op	op	op
Page 3	op	op	op	op	op	op	op

The configuration of 512B-page and 2KB-page NAND flash is similar, but there are some differences that need attention:

The size of the main area in each page is 512B, and that of the spare area is 16B Therein, the main area is divided into two 256B areas, each of which is addressed by A0~A7. In read and write operations, commands 0x00, 0x01 and 0x50 are sent to choose which 256B area or spare area (Don't care about the software; the hardware selects automatically, for example, when the configuration NAND controller writes 0x100, the hardware will automatically send it to high 256B area).
Transmit address command sequence is as follows:

	I/O	0	1	2	3	4	5	6	7
Column1	1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
Row1	2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16
Row2	3rd Cycle	A17	A18	A19	A20	A21	A22	A23	A24
Row3（注）	4th Cycle	A25	A26	*L	*L	*L	*L	*L	*L

(Notes: when the capacity of Nand flash is 64Mb, 128Mb and 256Mb, their corresponding largest column addresses of ADDR_R are A22, A23 and A24 respectively. Only address commands of Column1 and Row1~2 are sent three times, and Row3 won't be sent; when the capacity is 512Mb and 1Gb, Row3 needs to be sent.
4K/8K page- and 2K page-configurations are the same. The 4K page configuration has 4KB main area and 128B spare area; the 8K page configuration has 8KB main area and 640B spare area. Need to transmit five address commands.

20.4 Examples of Nand-flash Read and Write Operations

The "command valid" bit of the register can't be set simultaneously with other read and write enable bits. Only after the operation is set, can 'command valid' bit is set.
For example, to read the data of Main area, the operation is divided into two steps:
a. firstly, NAND_CMD = 0x102
b. Then, NAND_CMD = 0x103

20.5 NAND ECC Description

The hardware integrates ECC function, and ECC adopts the RS (204,188) method to encode and decode. But in software configuration, attention should be paid to the following:

1. In reading and writing NAND, 0 is recommended for the internal address (ADDR_C) of Page;
2. In each PAGE, NAND has 2048Bytes. After coding and decoding by RS (204,188), only the first 2040Bytes will be used, and 8 bytes will not; after the adoption of ECC, the NAND utilization rate is 188/204;
3. In operand configuration, in operating one page, the op_num in NAND is configured to multiples of 204 (in the unit of byte); in DMA configuration, the operand is the multiples of 47(188/4) (in the unit of word).
4. ECC operation and OOB operation may be separated. For example, after one page finishes ECC read/write, its OOB can be operated.
After the completion of ECC operation, all contents can be read back by common way, including original data and the data added by ECC check (the configuration operand op_num and DMA are the same). Check ability: 8 bytes may be corrected at most, and 1-8 bits may go wrong among those Bytes.
64bits are wrong in the first line of data, just equal to 8 bytes, which can be corrected; although 9bits are wrong in the last of data, and scatter among 9Bytes, which can't be corrected.

Original data (204Bytes)	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	...	
Data 1	00	00	00	00	00	00	00	00	ff	ff	ff	ff	…	Correctable
Data 2	1	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	…	Correctable
Data 3	fe	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	…	Correctable
Data 4	1	2	3	4	5	6	07	08	ff	ff	ff	ff	…	Correctable
Data 5	fe	fe	fe	fe	fe	fe	fe	fe	fe	ff	ff	ff	…	Uncorrectable

20.6 NAND BOOT Description

The NAND BOOT supports the NAND flash boot in 512B, 2K page, 4K page and 8K page. Based on the capacity and pagesize of FLASH, the pull-up and pull-down resistors of NAND_D[7:6] are configured (they must correspond to each other, or it may die, etc.). This is shown in figure below:

NAND_D [7:6] nand _type	In NAND boot, configure the particle capacity of NAND flash

	11 indicates the capacity is equal to 2GB (2K page/4K page/8K page) 10 indicates the capacity is 1GB (2K page) 01 indicates the capacity is 512MB (512 Bytes page) 00: it indicates the capacity is low and equal to 256MB (512 Bytes page)

In NAND boot, 1K bytes will be fetched from Page 0 for the chip initialization. If it's 512B, two pages will be read; if it's 2K page or larger, 1K bytes will be read. The system initial code needs to start from 0 byte from Page 0.

Through the pulling up and down of NAND_CLE, NAND BOOT may choose ECC boot or non-ECC boot. Their differences are: ECC adopts RS(204,188) code, and in ECC boot 1020 bytes are read, 940 bytes of which are valid data, and the rest coded data. (Notes: in ECC boot, 512B page isn't supported.)

21 RTC

21.1 Overview

Loongson 1C real-time clock unit can be configured after the main board is powered on, and after the main board is powered off, the unit still runs normally relying on the battery in main board. RTC unit only consumes several microwatts during operation.

RTC is driven by the external 32.768KHZ crystal oscillator, and after the frequency division by configurable frequency divider, this clock is used to count, and update hour, minute, second, day, month, and year. At the meantime, the clock is also used to generate various timing and counting interrupts.

RTC unit consists of counter and timer, and its architecture is shown in the figure below:

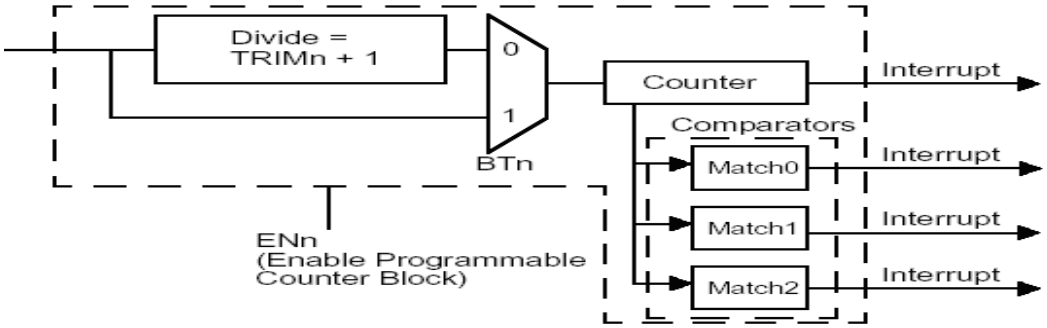

Figure 21-1 RTC block architecture diagram

21.2 Register Description

RTC module register is located in 0xbfe6_4000

In 16KB address space of -0xbfe6_7fff, its base address is 0xbfe6_4000, and the bit width of all registers is 32-bit.

21.2.1 Register address list

Name	Address	Bit width	RW	Description	Reset value
sys_toytrim	0xbfe6_4020	32	W	For the frequency division factor of 32.768kHz (Counter clock)	
sys_toywrite0	0xbfe6_4024	32	W	TOY low 32-bit value read-in	
sys_toywrite1	0xbfe6_4028	32	W	TOY high 32-bit value read-in	
sys_toyread0	0xbfe6_402C	32	R	TOY low 32-bit value read-out	
sys_toyread1	0xbfe6_4030	32	R	TOY high 32-bit value read-out	
sys_toymatch0	0xbfe6_4034	32	RW	TOY timer interrupt 0	
sys_toymatch1	0xbfe6_4038	32	RW	TOY timer interrupt 1	
sys_toymatch2	0xbfe6_403C	32	RW	TOY timer interrupt 2	
sys_rtcctrl	0xbfe6_4040	32	RW	TOY and RTC control register	
sys_rtctrim	0xbfe6_4060	32	RW	For the frequency division factor of 32.768kHz (Timer clock)	
sys_rtcwrite0	0xbfe6_4064	32	RW	RTC timer count write-in	
sys_rtcread0	0xbfe6_4068	32	RW	RTC timer counter read-out	
sys_rtcmatch0	0xbfe6_406C	32	RW	RTC clock timer interrupt 0	
sys_rtcmatch1	0xbfe6_4070	32	RW	RTC clock timer interrupt 1	

sys_rtcmatch2	0xbfe6_4074	32	RW	RTC clock timer interrupt 2	

Notes: after the reset of sys_toytrim and sys_rtctrim registers, their values can't be determined. If it's not necessary to divide the frequency of the external crystal oscillator, these two registers need clearing for the normal counting of the RTC module. The part marked in yellow in the above table doesn't exist in 1C2.

21.2.2 SYS_TOYWRITE0

English name: set up TOY counter low 32bits value
Register bit width: [31:0]
Offset: 0x24
Reset value: 0x00000000

Bit field	Bit field name	Access	Default	Description
31:26	TOY_MONTH	W		Months, ranging from 1 to 12
25:21	TOY_DAY	W		Days, ranging from 1 to 31
20:16	TOY_HOUR	W		Hours, ranging from 0 to 23
15:10	TOY_MIN	W		Minutes, ranging from 0 to 59
9:4	TOY_SEC	W		Seconds, ranging from 0 to 59
3:0	TOY_MILLISEC	W		0.1 seconds, ranging from 0 to 9

21.2.3 SYS_TOYWRITE1

English name: set up TOY counter low 32-bit value
Register bit width: [31:0]
Offset: 0x28
Reset value: 0x00000000

Bit field	Bit field name	Access	Default	Description
31:0	TOY_YEAR	W		Years, ranging from 0 to 99

21.2.4 SYS_TOYREAD0

English name: set up TOY counter low 32bits value
Register bit width: [31:0]
Offset: 0x2c
Reset value: 0x00000000

Bit field	Bit field name	Access	Default	Description
31:26	TOY_MONTH	R		Months, ranging from 1 to 12
25:21	TOY_DAY	R		Days, ranging from 1 to 31
20:16	TOY_HOUR	R		Hours, ranging from 0 to 23
15:10	TOY_MIN	R		Minutes, ranging from 0 to 59
9:4	TOY_SEC	R		Seconds, ranging from 0 to 59
3:0	TOY_MILLISEC	R		0.1 seconds, ranging from 0 to 9

21.2.5 SYS_TOYREAD1

English name: set up TOY counter low 32-bit value
Register bit width: [31:0]
Offset: 0x30
Reset value: 0x00000000

Bit field	Bit field name	Access	Default	Description
31:0	TOY_YEAR	R		Years, ranging from 0 to 99

21.2.6 SYS_TOYMATCH0/1/2 (no register in 1C2)

English name: TOY counter interrupt register 0/1/2
Register bit width: [31:0]
Offset: 0x34/38/3C
Reset value: 0x00000000

Bit field	Bit field name	Access	Default	Description
31:26	YEAR	Rw		Years, ranging from 0 to 16383
25:22	MONTH	Rw		Months, ranging from 1 to 12
21:17	DAY	Rw		Days, ranging from 1 to 31
16:12	HOUR	Rw		Hours, ranging from 0 to 23
11:6	MIN	Rw		Minutes, ranging from 0 to 59
5:0	SEC	Rw		Seconds, ranging from 0 to 59

21.2.7 SYS_RTCCTRL (no register in 1C2)

English name: RTC timer interrupt register 0/1/2
Register bit width: [31:0]
Offset: 0x40
Reset value: 0x00000000

Bit field	Bit field name	Access	Default	Description
31:24	Reserved	R	0	Reserved, set to 0
23	ERS	R	0	REN (bit13) write status
22:21	Reserved	R	0	Reserved, set to 0
20	RTS	R	0	Sys_rtctrim write status
19	RM2	R	0	Sys_rtcmatch2 write status
18	RM2	R	0	Sys_rtcmatch2 write status
17	RM0	R	0	Sys_rtcmatch0 write status
16	RS	R	0	Sys_rtcwrite write status
15	Reserved	R	0	Reserved, set to 0
14	BP	R/W	0	Bypass 32.768k oscillator 0: oscillator selection input; 1: GPIO8 is used to drive counter, which is the test mode. GPIO8 adopts the external clock or GPIO8 controller.
13	REN	R/W	0	0: RTC disabled; 1: RTC enabled
12	BRT	R/W	0	Bypass RTC frequency division 0: Normal operation; 1:RTC is directly driven by 32.768k crystal oscillator
11	TEN	R/W	0	0: TOY disabled; 1: TOY enabled
10	BTT	R/W	0	Bypass TOY frequency division 0: Normal operation; 1: TOY is directly driven by 32.768k oscillator
9	Reserved	R	0	Reserved, set to 0
8	EO	R/W	0	0: 32.768k oscillator disabled;

				1: 32.768k oscillator enabled
7	ETS	R	0	TOY enable write status
6	Reserved	R	0	Reserved, set to 0
5	32S	R	0	0:32.768k oscillator does not work; 1:32.768k oscillator works properly.
4	TTS	R	0	Sys_toytrim write status
3	TM2	R	0	Sys_toymatch2 write status
2	TM1	R	0	Sys_ toymatch1 write status
1	TM0	R	0	Sys_ toymatch0 write status
0	TS	R	0	Sys_toywrite write status

21.2.8 SYS_TOYMATCH0/1/2 (no register in 1C2)

English name: RTC timer interrupt register 0/1/2
Register bit width: [31:0]
Offset: 0x 6C/70/74
Reset value: 0x00000000

Bit field	Bit field name	Access	Default	Description
31:26	YEAR	RW		Years, ranging from 0 to 16383
25:22	MONTH	RW		Months, ranging from 1 to 12
21:17	DAY	RW		Days, ranging from 1 to 31
16:12	HOUR	RW		Hours, ranging from 0 to 23
11:6	MIN	RW		Minutes, ranging from 0 to 59
5:0	SEC	RW		Seconds, ranging from 0 to 59

22 SDIO Controller

22.1 Function Overview

Loongson 1C integrates one SDIO controller that is used for the read and write of SD Memory and SDIO, and supports the boot of Memory card. SDIO controller features are in the following:

- Be compatible with the specification of SD storage card (version 2.0)
- Be compatible with the specification of SDIO card (version 2.0)
- 8 words (32 bytes) data sending/receiving FIFO
- Expanded 256bits SD card status register
- 8 bits prescale logic (frequency=system clock /(p+1))
- DMA data transmission mode
- SD mode of 1-bit/4 bits (wide bus)

22.2 SDIO Protocol Overview

SDIO is a serial communication method, and master and slave devices can implement the transmission of data and status by message delivery. The below is the schematic diagram of writing multi-block data, and its process is as follows:

1. The master device sends the write command message to salve device by order wire.
2. After the slave device receives the message, it sends the acknowledgment message to slave device by order line.
3. After the master device receives the right acknowledge message, a data block (512K Byte or more) are sent to the slave device by data line and to test the busy status of data line.
2. After the slave device receives the right data, it enters into the programming state. Then, the data line is set to busy, and won't respond to the data request of master device.
5. From the master device detection to device programming, the next data block will be sent continuously.
6. After the master device sends the last data block, it sends the stop command to the slave device by command line. After the slave device receives the right response, the multi-block read and write operations are finished.

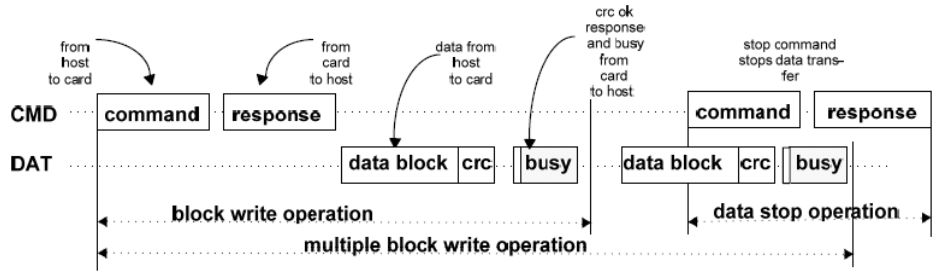

Figure 22-1 Schematic diagram of SD card multi-block write operation

The multi-block read operation is similar with the multi-block write operation (supplementary instructions).

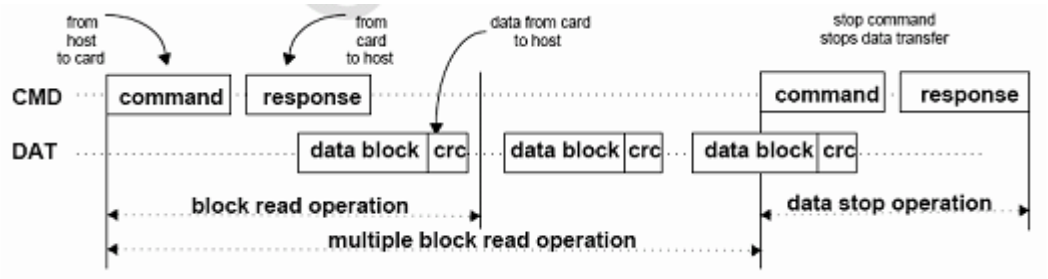

Figure 22-2 Schematic diagram of SD card multi-block read operation

Different commands have a uniform format. The format of general commands is shown in the table below, 1bit start bit, 1bit transmission direction bit, 6bit command sequence number, 32bit command parameter, 7bit CRC check bit and 1bit stop bit.

Table 22-1 Command format in SD mode

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	x	x	x	'1'
Description	start bit	transmission bit	command index	argument	CRC7	end bit

Therein, the command index corresponds to the command number, for example, cmdindex is 0 for command 0, and cmdindex is 37 for command 55. Parameters of different commands may be different. Please refer to SD protocol specification

22.3 Register Description

The register of SDIO controller is shown as follows:

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_con	0xbfe6c000	r/w	SDIO control register	0x0

sdi_con	Bit	Default values	Description
reserved	31:9	0x0	
soft_rst	8	0x0	Software reset, the entire module is reset. Hardware is automatically cleared after reset
reserved	7:0	0x0	
enclk	0	0x0	SD clock output enable

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_pre	0xbfe6c004	r/w	SDIO prescale register	0x1

sdi_pre	Bit	Default values	Description
reserved	31:8	0x0	
sdi_pre	7:0	0x1	SDIO clock prescale value, the output frequency =PCLK/prescale value

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_cmd_arg	0xbfe6c008	r/w	SDIO command parameter register	0x0

sdi_cmd_arg	Bit	Default values	Description
sdi_cmd_arg	31:0	0x0	Command parameter

Register name	Address	Read / Write (R / W)	Function description	Reset value

sdi_cmd_con	0xbfe6c00c	r/w	SDIO command control register	0x0

sdi_cmd_con	Bit	Default values	Description
reserved	31:18	0x0	
func_num_abort	17: 15	0x0	When the function number of SDIO card interrupt is used fo multi-block read and write, the hardware will send the sto command automatically. If auto_stop_en is 0, this bit i insignificant.
sdio_en	14	0x0	SDIO enable signal. When used for multi-block read and write, the hardware will send the stop command automatically. If the bit is 1, CMD52 is sent; if the bit is 0, CMD12 is sent. If auto_stop_en is 0, this bit is insignificant.
check_on	13	0x0	Check the CRC or not, significant at 1
auto_stop_en	12	0x0	Hardware automatically sends a stop command. In multi-block rea and write, does the hardware send the stop command automatically? If the bit is 1, it's significant.
reserved	11	0x0	
long_rsp	10	0x0	Is it the 136-bit long response? If the bit is 1, it's the long message reply.
wait_rsp	9	0x0	It decides whether the host waits for the response. If the bit is 1, it indicates waiting for message reply.
CMST	8	0x0	When the bit is set to 1, the command starts, and the hardware is cleared automatically after the command ends.
cmd_index	7:0	0x0	Command index with initial 2 bits (8bits in total)

Register name	**Address**	**Read / Write (R / W)**	**Function description**	**Reset value**
sdi_cmd_sta	0xbfe6c010	ro	SDIO command status register	0x0

sdi_cmd_sta	Bit	Default value	Description
reserved	31:13	0x0	
cmd_sent_fin	14	0x0	Flag bit of the command sending (including response) finished. When the bit is 1, it indicates that the command is sent and the response is made.
auto_stop	13	0x0	Flag bit of hardware sending stop command automatically. When the bit is 1, it indicates that the hardware sends stop command automatically, and when it's 0, it indicates the hardware sends does not stop command automatically
rsp_crc_err	12	0x0	Response CRC error. Received response CRC error. When the bit is 1, it indicates responding CRC error, and when it's 0, it indicates no

			CRC error is found.
cmd_end	11	0x0	Command sending finished (indifferent to concern). When the bit is 1, it indicates command sending finished, and when it's 0, it indicates command sending unfinished.
cmd_tout	10	0x0	Command timeout. Command response timeout (64 clock periods) or $R1_b$ command, busy waiting command. When the bit is 1, it indicates response timeout, and when it's 0, it indicates no timeout.
rsp_fin	9	0x0	Response finished, and return message received from equipment. When the bit is 1, it indicates response finished, and when the bit is 0, it indicates response unfinished.
cmd_on	8	0x0	Flag bit of command transmission. When the bit is 1, it indicates transmission under way, and when it's 0, it indicates the transmission is finished.
rsp_index	7:0	0x0	Response index with initial 2 bits returned from equipment (8bits in total)

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_rsp0	0xbfe6c014	ro	SDIO command response register 0	0x0

sdi_cmd_arg	Bit	Default values	Description
sdi_rsp0	31:0	0x0	Card status [31:0] (short), card status [127:96] (long) see sdi_cmd_con[10] for the configuration of long response

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_rsp1	0xbfe6c018	ro	SDIO command response register 1	0x0

sdi_cmd_arg	Bit	Default values	Description
sdi_rsp1	31:0	0x0	Unused (short), card status [95:64] (long) see sdi_cmd_con[10] for the configuration of long response

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_rsp2	0xbfe6c01c	ro	SDIO command	0x0

			response register 2	

sdi_cmd_arg	Bit	Default values	Description
sdi_rsp2	31:0	0x0	Unused (short), card status [63:32] (long) see sdi_cmd_con[10] for the configuration of long response

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_rsp3	0xbfe6c020	ro	SDIO command response register 3	0x0

sdi_cmd_arg	Bit	Default values	Description
sdi_rsp3	31:0	0x0	Unused (short), card status [31:0] (long) see sdi_cmd_con[10] for the configuration of long response

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_dtimer	0xbfe6c024	r/w	SDIO command data timeout register	0x0

sdi_dtimer	Bit	Default values	Description
reserved	31:24	0x0	
sdi_dtimer	23:0	0x0	Data timeout count value uses the clock count after frequency division

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_bsize	0xbfe6c028	r/w	SDIO block size register	0x0

sdi_bsize	Bit	Default values	Description
reserved	31:23	0x0	
sdi_bsize	11:0	0x0	Block size value (0 to 4095)

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_dat_con	0xbfe6c02c	r/w	SDIO data control register	0x0

sdi_dat_con	Bit	Default values	Description
reserved	31:15	0x0	
resume_rw	20	0x0	SDIO suspend and resume reading and writing flag bit. When the bit is 1, the previous write operations are recovered after SDIO suspension; when the bit is 0, previous read operations are recovered.
IO_resume	19	0x0	SDIO recovery request. After the SDIO

			device enters into the suspended state, 1 is written to this bit. After 0 is written to IO_suspend, SDIO device recovers previous operations.
IO_suspend	18	0x0	SDIO suspending request. After 1 is written to this bit, the controller will send CMD52 command in right time, and notify SDIO device to enter into the suspended state. Write 0 in this bit when resuming operation
RwaitReq	17	0x0	Read pending request After 1 is written to the bit, the controller will pull down DAT2 in right time, and notify SDIO device to enter into the read waiting state. Write 0 to recover the previous read operation.
wide_mode	16	0x0	Bit width select bit. When the bit is 1, it indicates t he four-wire mode; when the bit is 0, it indicates the single-line mode.
DMA_en	15	0x0	DMA enable When the bit is 1, it indicates DMA enable; when the bit is 0, it indicates DMA disable.
DTST	14	0x0	When 1 is written to the bit, the data transfer begins, and the hardware is cleared after the data transfer ends.
reserved	13:12	0x0	
blk_num	11:0	0x0	The number of blocks for reading and writing operations

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_dat_cnt	0xbfe6c030	r/w	SDIO data counter	0x0

sdi_dat_cnt	Bit	Default values	Description
reserved	31:24	0x0	
blk_num_cnt	23:12	0x0	Current number of bytes of transmission blocks
blk_cnt	11:0	0x0	Current number of transmission blocks

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_dat_sta	0xbfe6c034	ro	SDIO data status register	0x0

sdi_dat_sta	Bit	Default values	Description
reserved	31:11	0x0	
suspend_on	16	0x0	When the bit is 1, it indicates in suspended status.
rst_suspend	15	0x0	When the bit is 1, it indicates .in suspended reset After the SDIO device is suspended, the controller resets FIFO and DMA requests.
R1b_tout	14	0x0	When the bit is 1, it indicates R1b

			command timeout.
data_start	13	0x0	When the bit is 1, it indicates data transmission starting
R1b_fin	12	0x0	Test the completion of the command with busy state When the command with busy state is sent, the bit is 0; when the busy state ends, the bit becomes 1.
auto_stop	11	0x0	When the bit is 1, it indicates the hardware is sending the stop command automatically.
reserved	10	0x0	
r_wait_req	9	0x0	Reading waiting to happen. Send the read waiting request signal to SDIO card.
SDIO_int	8	0x0	SDIO interrupt flag bit. When the bit is 1, it indicates interrupt detection
crc_sta	7	0x0	After the data transfer, CRC error is returned from the device
dat_crc	6	0x0	Data receiving CRC errors
dat_tout	5	0x0	Data transmission timeout. When the bit is 1, it indicates data timeout
dat_fin	4	0x0	Data transmission end flag bit. When the bit is 1, it indicates data transmission end
busy_fin	3	0x0	Busy end flag bit (such as programming). When the bit is 1, it indicates busy end
prog_err	2	0x0	Programming error flag bit. When the bit is 1, it indicates the wrong programming.
tx_dat_on	1	0x0	In Tx data transfer, when the bit is 1, it indicates sending; when the bit is 0, it indicates sending completes.
rx_dat_on	0	0x0	In rX data acceptance, when the bit is 1, it indicates receiving; when the bit is 0, it indicates receiving completes.

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_fifo_sta	0xbfe6c038	ro	SDIOFIFO Status register	0x0

sdi_fifo_sta	Bit	Default values	Description
reserved	31:12	0x0	
tx_full	11	0x0	tx fifo full flag bit
tx_empty	10	0x0	tx fifo empty flag bit
reserved	9	0x0	
rx_full	8	0x0	rx fifo full flag bit
rx_empty	7	0x0	rx fifo empty flag bit
reserved	6:0	0x0	

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_int_msk	0xbfe6c03c	r/c	SDIO interrupt register	0x0

sdi_int_msk	Bit	Default values	Description

reserved	31:10	0x0	
R1b_fin_int	9	0x0	Detest busy end interrupt, 1 is written to the bit for clearing.
rsp_crc_int	8	0x0	The command responds to CRC error interrupt, and 1 is written to the bit for clearing.
cmd_tout_int	7	0x0	Command timeout interrupt, 1 is written to the bit for clearing.
cmd_fin_int	6	0x0	Number of command transmission completion interrupt, hardware clearing
SDIO_int	5	0x0	Detest SDIO interrupt, and 1 is written to the bit for clearing.
prog_err_int	4	0x0	SD card programming error interrupt, and 1 is written to the bit for clearing
crc_sta_int	3	0x0	After the data is sent, CRC error interrupt is returned from device, write 1 and clear
dat_crc_int	2	0x0	The data receives CRC error interrupt, write 1 and clear
dat_tout_int	1	0x0	Data timeout interrupt, and 1 is written to the bit for clearing
dat_fin_int	0	0x0	Data interrupt completion, hardware clearing

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_dat	0xbfe6c040	ro	SDIO command data register	0x0

sdi_dat	Bit	Default values	Description
sdi_dat	31:0	0x0	SDIO controller sends or receives data (used DMA operation)

Register name	Address	Read / Write (R / W)	Function description	Reset value
sdi_int_en	0xbfe6c064	r/w	SDIO interrupt enable register	0x0

sdi_int_en	Bit	Default values	Description
reserved	31:10	0x0	
R1b_fin_int_en	9	0x0	Busy finish interrupt enable. When the bit is 1, it's significant.
rsp_crc_int_en	8	0x0	Command response CRC error interrupt enable. When the bit is 1, it's significant.
cmd_tout_int_en	7	0x0	Command timeout interrupt enable, significant at 1
cmd_fin_int_en	6	0x0	Data command send finish interrupt enable. When the bit is 1, it's significant.
SDIO_int_en	5	0x0	SDIO interrupt enable. When the bit is 1, it's significant.
prog_err_int_en	4	0x0	SD card programming error interrupt enable. When the bit is 1, it's significant.
crc_sta_int_en	3	0x0	Return CRC error interrupt enable after the data transfer. When the bit is 1, it's significant.

dat_crc_int_en	2	0x0	Data receive CRC error interrupt enable. When the bit is 1, it's significant.
dat_tout_int_en	1	0x0	Data timeout interrupt enable, significant at 1
dat_fin_int_en	0	0x0	Data completion interrupt enable, significant at 1

22.4 Software Programming Instructions

22.4.1 SD Memory card software programming instructions

If SD Memory card wants to operate normally, it must be initialized first. The initialization process needs to send different command sequences to configure the slave device. Initialization process diagram as follows:

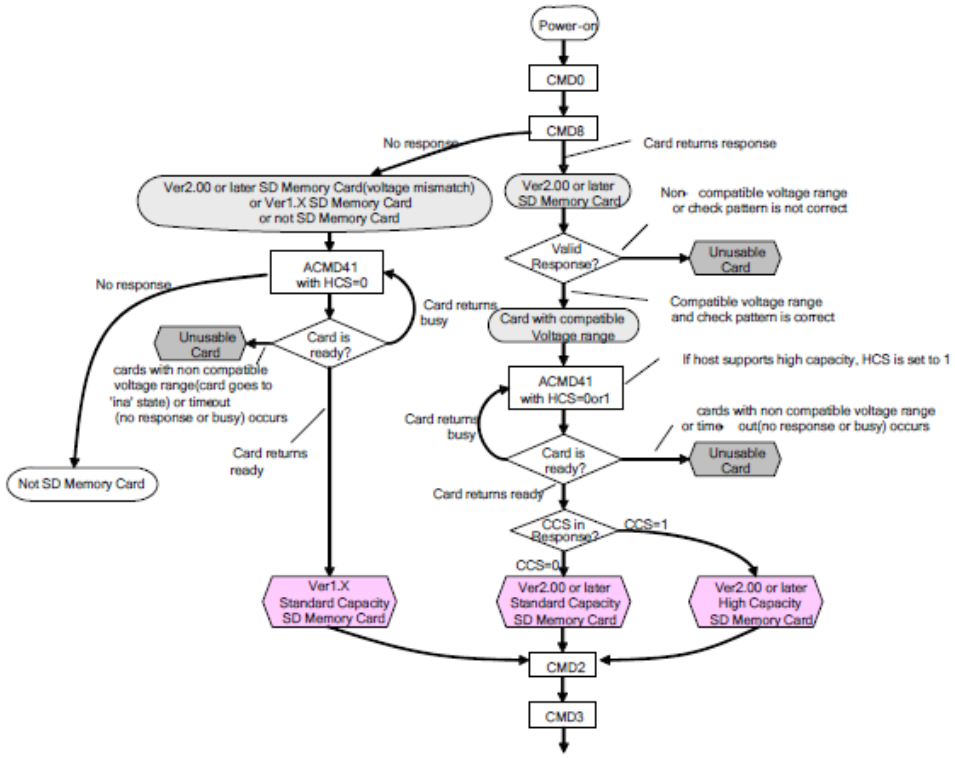

Figure 22-3 Schematic diagram of SD Memory card initialization process

Normal work can be carried out after initialization completion.

Configuration register process is as follows:

1. Configure sdi_con, enable output clock
2. Configure sdi_pre, set a frequency division factor, and if the time sequence isn't satisfied, the output direction clock is set to adjust the time sequence.
3. Configure sdi_int_en, enable command and data completion and other interrupts.
4. According to the above initialization process, the configuration register where initialization controller sends command as follows:
   - Based on the sent command, the cmd_arg register is configured.
   - Configure cmd_con register, send command
   - Read sdi_int_msk register, and check if the transfer is finished, and if there is an error
   - If necessary, read the sdi_rsp register

Initialization process is as follows:
CMD0→CMD8→ACMD41(namely, CMD55→CMD41) →CMD2→CMD3→CMD7→ACMD6 (if 4bit data line is used for transfer)
5. Before the data operation, it's necessary to configure Bsize register and Dtimer register.

6. For the data operation, it's necessary to configure DMA, configure dat_con register and DMA (Notes: In read operation, configure DMA first, and in write operation, configure dat_con first)
7. Read sdi_int_msk register, and check if the transfer is finished, and if there is an error
8. Without error, one data transfer is finished, and it doesn't need the software to send stop command.

22.4.2 SDIO card software programming instructions

The initialization process of SDIO card is different from that of SD memory card, and it's initialized as follows:

1. Configure sdi_con, enable output clock
2. Configure sdi_pre, set one frequency division factor. If the time sequence isn't satisfied, the output inversion is set.
3. Clock to adjust timing sequence.
4. Configure sdi_int_en, enable command and data completion and other interrupts.
5. Initialization process is as follows: Configuration register process for transmitting command is as follows:

- Based on the sent command, the cmd_arg register is configured.
- Configure cmd_con register, send command
- Read sdi_int_msk register, and check if the transfer is finished, and if there is an error
- If necessary, read the sdi_rsp register

The initialization process is shown as follows (the CCCR operation)

6. CMD52 (reset) →CMD5 (after powered on) →CMD3 (obtain RCA) →CMD7 (select the corresponding RCA card) →CMD52 (configure whether to use 4bit data line transmission) →CMD52 (configure the block size of read and write data) →CMD52 (open IO interrupt enable) it's necessary to configure Bsize register and Dtimer register before row data operation.
7. For the data operation, it's necessary to configure DMA, configure dat_con register and DMA (Notes: In read operation, configure DMA first, and in write operation, configure dat_con first)
8. In sending the command of read and write data, if the hardware is required to send stop command automatically, it's necessary to configure auto_stop and sdio_en. In reading and writing data, it's necessary to read and write Function, configure the corresponding FBR pointer register, and then send multi-block read and write (CMD53) or single-block read and write (CMD52) command to read and write.
9. Read sdi_int_msk register, and check if the transfer is finished, and if there is an error
10. Without error, one data transfer is finished, and it doesn't need the software to send stop command.
11. If the IO interrupt is detected, the controller will enable the interrupt triggering response, but will not stop the current operation.
12. For the read waiting, the controller will pull down DAT2 in right time, and notify the SDIO card to stop sending data. Thus, if it's under the process of data transfer, the controller may send the wait signal after the previous data block transfer ends, and it won't receive the next block data.
13. 13 For the suspending and resuming operations. Suspend and nest may occur, for example, operation 1 is suspended because operation 2 interrupts, and then operation 2 is suspended because operation 3 interrupts. In suspension, the interrupt field requires the software to save(such as read and write flag bit, number of current transmission block, address and so on), and starts the PUSH operation. In recovery, the software is pulled in corresponding sequence.

23 CAN Controller

23.1 Overview

1C integrates two ways of CAN interface controllers CAN bus is the serial bus made up of transmitter data line TX and receiver data line RX to transmit and receive data. The bidirectional transfer is conducted between devices, and the highest transfer rate is 1Mbps

The interrupt of two CAN bus controllers is connected to the first group of interrupt control registers. Therein, can0 interrupt corresponds to bit6, and can1 interrupt to bit7. Refer to description in Chapter 15.

The register base address of CAN0 bus controller is 16KB at the beginning of 0xbfe5_0000.

The register base address of CAN1 bus controller is 16KB at the beginning of 0xbfe5_4000.

23.2 CAN Controller Architecture

The figure below is the architecture of CAN master controller, and main modules include APB bus interface, bit stream processing unit, bit time sequence logic, error management logic, receiving filtering, and data buffer cache.

- APB bus interface: receive APB bus command and return data.
- Bit stream processing unit: implement the control of data stream between transmitter buffer, receiver FIFO and CAN bus, and performs functions such as error detection, bus arbitration, data filling and error handling.
- Bit time sequence logic: monitor the serial CAN bus and handle the bit time sequence related to the bus. In addition, it provides the programmable time quantum to compensate the propagation delay time, phase switch (for example, due to oscillation drift) and define the sampling point and sampling times within the time of one bit.
- Error management logic: judge the transmitted CRC error and count errors.
- Receiving filtering: compared the received identification codes to decide whether to receive the message or not.
- Data buffer cache: the receiving buffer is the interface between acceptance filter and CPU, and is also used to store messages received from CAN bus. As one window of FIFO (64 bytes long) , the receive buffer (13 bytes) may be accessed by CPU.

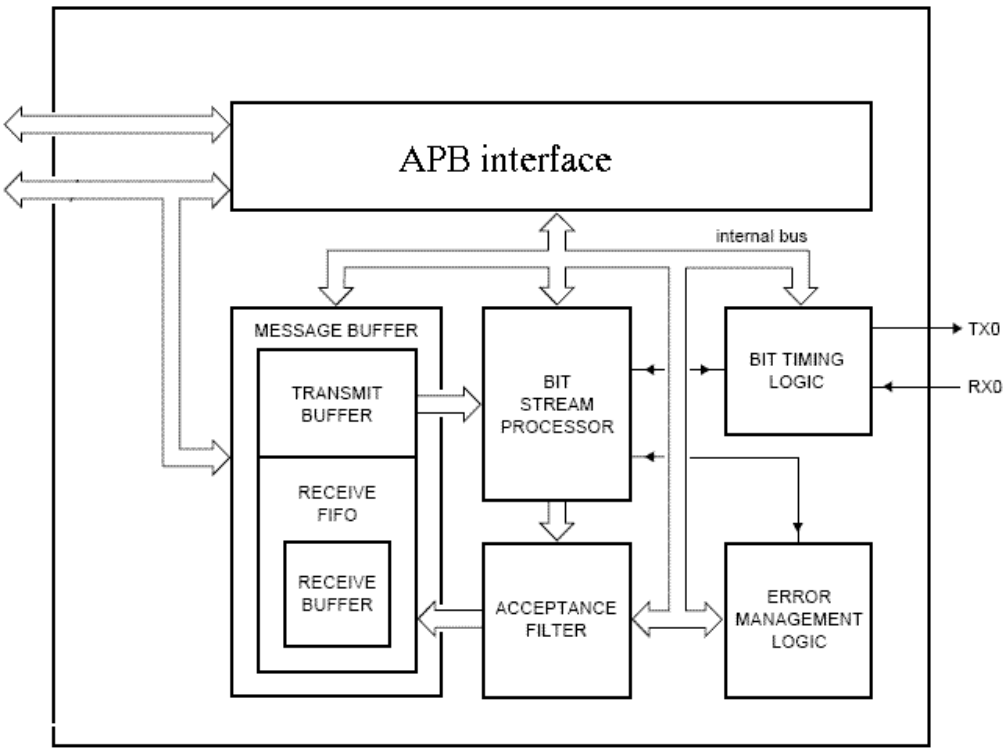

Figure 23-1 CAN master controller architecture

CAN supports two operating modes: standard mode and expansion mode. The operating mode is selected through CAN mode in command register. Reset default is the standard mode.

23.3 Standard Mode

23.3.1 Standard mode address list

The address area includes the control segment and message buffer. In initial loading, the control segment may be programmed to configure communication parameters, and the message to be transmitted will be written in send buffer. After receiving the message, the microcontroller will read the received message from receive buffer, and then release the space for next application.
After the initial loading, the acceptance code and acceptance mask of register, 0 and 1 of bus timing register, and output control can't be changed. Only when the reset bit of control register is set high, can these registers be accessed. In different modes of reset mode and operating mode, the access register is different. After the hardware reset or controller drops, the bus status of status register will enter into the reset mode automatically. The operating mode is activated by the reset request of setting control register.

CAN address	field	Operating mode		Reset mode	
		Read	Write	Read	Write
0	Control	Control	Control	Control	Control
1		FF	Commands	FF	Commands
2		Status	—	Status	—
3		FF	—	Interrupt	—
4		FF	—	Acceptance code	Acceptance code
5		FF	—	Acceptance mask	Acceptance mask
6		FF	—	Bus timing 0	Bus timing 0
7		FF	—	Bus timing 1	Bus timing 1
8		Reserved	Reserved	Reserved	Reserved
9		Reserved	Reserved	Reserved	Reserved
10		ID (10-3)	ID (10-3)	FF	—
11		ID (2-0), RTR, DLC	ID (2-0), RTR, DLC	FF	—
12		Data byte 1	Data byte 1	FF	—
13		Data byte 2	Data byte 2	FF	—
14		Data byte 3	Data byte 3	FF	—
15		Data byte 4	Data byte 4	FF	—
16		Data byte 5	Data byte 5	FF	—
17		Data byte 6	Data byte 6	FF	—
18		Data byte 7	Data byte 7	FF	—
19		Data byte 8	Data byte 8	FF	—
20		ID (10-3)	ID (10-3)	FF	—
21		ID (2-0), RTR, DLC	ID (2-0), RTR, DLC	FF	—
22		Data byte 1	Data byte 1	FF	—
23		Data byte 2	Data byte 2	FF	—
24		Data byte 3	Data byte 3	FF	—
25		Data byte 4	Data byte 4	FF	—
26		Data byte 5	Data byte 5	FF	—
27		Data byte 6	Data byte 6	FF	—
28		Data byte 7	Data byte 7	FF	—
29		Data byte 8	Data byte 8	FF	—

23.3.2 Control register (CTR)

English name: control register
Register bit width: [7:0]
Offset: 0x00
Reset value: 0x01

The reading value of this bit is always logic 1. In hard boot or when the bus status bit set to 1 (bus shutdown), the reset request bit is set to 1. If these bits are accessed by software, its value will change and influence the next rising edge of the internal clock. During the external reset, the microprocessor can't set the reset request bit to 0. If the reset request bit is set to 0, the microprocessor must check the bit and guarantee the external reset pin isn't low. The change in reset request bit is synchronous with internal frequency division clock. Read reset request bit, and you can find such synchronous state.
After the reset request bit is set to 0, the controller will wait.
a) One bus idle signal (11 weak bit), if the previous reset request is hardware rest or CPU initial reset.
b) 128 buses are idle, if the previous reset request is caused by initialization bus before CAN controller reenters the bus startup mode.

Bit field	Bit field name	Bit width	Access	Description
7: 5	Reserve	3	—	Reserved
4	OIE	1	Rw	Overflow interrupt enable
3	EIE	1	Rw	Error interrupt enable
2	TIE	1	Rw	Transmit interrupt enable
1	RIE	1	Rw	Receive interrupt enable
0	RR	1	Rw	Reset request

23.3.3 Command register (CMR)

English name: Command register
Register bit width: [7:0]
Offset: 0x01
Reset value: 0x00

For microcontroller, the command register is the write-only memory, and if the address is read, the returned value is 1111 1111.

Bit field	Bit field name	Bit width	Access	Description
7	EFF	1	W	Extension mode
6: 5	Reserve	2	—	Reserved
4	GTS	1	W	sleep
3	CDO	1	W	Clear data overflow
2	RRB	1	W	Release receiving buffer
1	AT	1	W	Stop transmitting
0	TR	1	W	RTS (Request to send)

23.3.4 Status register (SR)

English name: Status register
Register bit width: [7:0]
Offset: 0x02
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	BS	1	R	Bus status

6	ES	1	R	Faulted state
5	TS	1	R	Send state
4	RS	1	R	Receive state
3	TCS	1	R	Send completed state
2	TBS	1	R	Transmit buffer state
1	DOS	1	R	Data overflow state
0	RBS	1	R	Receive buffer status

23.3.5 Interrupt register (IR)

English name: Interrupt register
Register bit width: [7:0]
Offset: 0x03
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7: 5	Reserved	1	R	Reserved
4	WUI	1	R	Wake-up interrupt
3	DOI	1	R	Data overflow interrupt
2	EI	1	R	Error interrupt
1	TI	1	R	Send interrupt
0	RI	1	R	Receive interrupt

23.3.6 Acceptance Code Register (ACR)

English name: Acceptance code register
Register bit width: [7:0]
Offset: 0x04
Reset value: 0x00
In reset, the register may be read and written.

Bit field	Bit field name	Bit width	Access	Description
7:0	AC	8	RW	ID acceptance code

23.3.7 Acceptance Mask Register (AMR)

English name: Acceptance mask register
Register bit width: [7:0]
Offset: 0x05
Reset value: 0x00
Acceptance code bit AC is equal to high 8bits ID.10-ID.3 of message identification code, and when it corresponds to the phase of acceptance mask bit or is 1, the data may be accepted. In reset, the register may be read and written.

Bit field	Bit field name	Bit width	Access	Description
7:0	AM	8	Rw	ID mask bit

23.3.8 Transmit buffer list

The buffer is used to store the message that the microprocessor requires CAN controller to send, and it's divided into descriptor area and data area. The read/write of buffer can only be sent by microcontroller in operating mode, and in reset mode the read value is always FF.

Address	Area	Name	Data bit
10		ID byte 1	ID (10-3)

11		ID byte 2	ID (2-0), RTR, DLC
12		TX data 1	TX data 1
13		TX data 2	TX data 2
14		TX data 3	TX data 3
15		TX data 4	TX data 4
16		TX data 5	TX data 5
17		TX data 6	TX data 6
18		TX data 7	TX data 7
19		TX data 8	TX data 8

23.3.9 Receive buffer list

The configuration of receive buffer and send buffer is the same, but the address is changed to 20-29.

23.4 Extension Mode

23.4.1 Extension mode address table

CAN address	Operating mode		Reset mode	
	Read	Write	Read	Write
0	Control	Control	Control	Control
1	0	Commands	0	Commands
2	Status	—	Status	—
3	Interrupt	—	Interrupt	—
4	Interrupt enable	Interrupt enable	Interrupt enable	Interrupt enable
5	—	—	Acceptance mask	Acceptance mask
6	Bus timing 0	—	Bus timing 0	Bus timing 0
7	Bus timing 1	—	Bus timing 1	Bus timing 1
8	Reserved	Reserved	Reserved	Reserved
9	Reserved	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved	Reserved
11	Arbitration lost capture	—	Arbitration lost capture	—
12	Error code capture	—	Error code capture	—
13	Error alarm limit	—	Error alarm limit	—
14	RX error counter	—	RX error counter	—
15	TX error counter	—	TX error counter	—
16	RX frame information	TX frame information	Acceptance Code 0	Acceptance Code 0
17	RX ID 1	TX ID 1	Acceptance Code 1	Acceptance Code 1
18	RX ID 2	TX ID 2	Acceptance Code 2	Acceptance Code 2
19	RX ID 3	TX ID 3	Acceptance Code 3	Acceptance Code 3
20	RX ID 4	TX ID 4	Acceptance mask 0	Acceptance mask 0
21	RX data 1	TX data 1	Acceptance mask 1	Acceptance mask 1
22	RX data 2	TX data 2	Acceptance mask 2	Acceptance mask 2
23	RX data 3	TX data 3	Acceptance mask 3	Acceptance mask 3
24	RX data 4	TX data 4	—	—
25	RX data 5	TX data 5	—	—
26	RX data 6	TX data 6	—	—
27	RX data 7	TX data 7	—	—
28	RX data 8	TX data 8	—	—

29	RX message counter	—	RX message counter	—

23.4.2 Mode register (MOD)

English name: Mode register
Register bit width: [7:0]
Offset: 0x00
Reset value: 0x01

The reading value of this bit is always logic 1. In hard boot or when the bus status bit set to 1 (bus shutdown), the reset request bit is set to 1. If these bits are accessed by software, its value will change and influence the next rising edge of the internal clock. During the external reset, the microprocessor can't set the reset request bit to 0. If the reset request bit is set to 0, the microprocessor must check the bit and guarantee the external reset pin isn't low. The change in reset request bit is synchronous with internal frequency division clock. Read reset request bit, and you can find such synchronous state.
After the reset request bit is set to 0, the controller will wait.
a) One bus idle signal (11 weak bit), if the previous reset request is hardware rest or CPU initial reset.
b) 128 buses are idle, if the previous reset request is caused by initialization bus before CAN controller reenters the bus startup mode.

Bit field	Bit field name	Bit width	Access	Description
7: 5	Reserve	3	—	Reserved
4	SM	1	Rw	Sleep mode
3	AFM	1	Rw	Single / Dual filter mode
2	STM	1	Rw	Normal operating mode
1	LOM	1	Rw	Listen mode
0	RM	1	Rw	Reset mode

23.4.3 Command register (CMR)

English name: Command register
Register bit width: [7:0]
Offset: 0x01
Reset value: 0x00

For microcontroller, the command register is the write-only memory, and if the address is read, the returned value is 1111 1111.

Bit field	Bit field name	Bit width	Access	Description
7	EFF	1	W	Extension mode
6: 5	Reserve	2	—	Reserved
4	SRR	1	W	Self receiving request
3	CDO	1	W	Clear data overflow
2	RRB	1	W	Release receiving buffer
1	AT	1	W	Stop transmitting
0	TR	1	W	RTS (Request to send)

23.4.4 Status register (SR)

English name: Status register
Register bit width: [7:0]
Offset: 0x02
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	BS	1	R	Bus status
6	ES	1	R	Faulted state
5	TS	1	R	Send state
4	RS	1	R	Receive state
3	TCS	1	R	Send completed state
2	TBS	1	R	Transmit buffer state
1	DOS	1	R	Data overflow state
0	RBS	1	R	Receive buffer status

23.4.5 Interrupt register (IR)

English name: Interrupt register
Register bit width: [7:0]
Offset: 0x03
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	BEI	1	R	Bus error interrupt
6	ALI	1	R	Arbitration lost interrupt
5	EPI	1	R	Error passive interrupt
4	WUI	1	R	Wake-up interrupt
3	DOI	1	R	Data overflow interrupt
2	EI	1	R	Error interrupt
1	TI	1	R	Send interrupt
0	RI	1	R	Receive interrupt

23.4.6 Interrupt enable register (IER)

English name: Interrupt enable register
Register bit width: [7:0]
Offset: 0x04
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	BEIE	1	RW	Bus error interrupt enable
6	ALIE	1	RW	Arbitration lost interrupt enable
5	EPIE	1	RW	Error passive interrupt enable
4	WUIE	1	RW	Wake-up interrupt enable
3	DOIE	1	RW	Data overflow interrupt enable
2	EIE	1	RW	Error interrupt enable
1	TIE	1	RW	Transmit interrupt enable
0	RIE	1	RW	Receive interrupt enable

23.4.7 Arbitration Loss Capture Register (IER)

English name: Arbitration lost capture register
Register bit width: [7:0]
Offset: 0xB
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7: 5	—	3	R	Reserved
4	BITNO4	1	R	Fourth bit
3	BITNO3	1	R	Third bit
2	BITNO2	1	R	Second bit
1	BITNO1	1	R	First bit
0	BITNO0	1	R	Zero bit

Bit					Decimal value	Function
0	0	0	0	0	0	Arbitration lost in the ID code bit1
0	0	0	0	1	1	Arbitration lost in the ID code bit 2
0	0	0	1	0	2	Arbitration lost in the ID code bit3
0	0	01	1		3	Arbitration lost in the ID code bit4
0	0	1	0	0	4	Arbitration lost in the ID code bit5
0	0	1	0	1	5	Arbitration lost in the ID code bit6
0	0	1	1	0	6	Arbitration lost in the ID code bit7
0	0	1	1	1	7	Arbitration lost in the ID code bit8
0	1	0	0	0	8	Arbitration lost in the ID code bit9
0	1	0	0	1	9	Arbitration lost in the ID code bit10
0	1	0	1	0	10	Arbitration lost in the ID code bit11
0	1	0	1	1	11	Arbitration lost in SRTR bit
0	1	1	0	0	12	Arbitration lost in IDE bit
0	1	1	0	1	13	Arbitration lost in the ID code bit12
0	1	1	1	0	14	Arbitration lost in the ID code bit13
0	1	1	1	1	15	Arbitration lost in the ID code bit14
1	0	0	0	0	16	Arbitration lost in the ID code bit15
1	0	0	0	1	17	Arbitration lost in the ID code bit16
1	0	0	1	0	18	Arbitration lost in the ID code bit17
1	0	0	1	1	19	Arbitration lost in the ID code bit18
1	1	1	0	0	20	Arbitration lost in the ID code bit19
1	1	1	0	1	21	Arbitration lost in the ID code bit 20
1	1	1	1	0	22	Arbitration lost in the ID code bit21
1	1	1	1	1	23	Arbitration lost in the ID code bit22
1	0	0	0	0	24	Arbitration lost in the ID code bit 23
1	0	0	0	1	25	Arbitration lost in the ID code bit 24
1	0	0	1	0	26	Arbitration lost in the ID code bit 25
1	0	0	1	1	27	Arbitration lost in the ID code bit26
1	1	1	0	0	28	Arbitration lost in the ID code bit 27
1	1	1	0	1	29	Arbitration lost in the ID code bit 28
1	1	1	1	0	30	Arbitration lost in the ID code bit 29
1	1	1	1	1	31	Arbitration lost in RTR bit

23.4.8 Error Alarm Limit Register (EMLR)

English name: Error alarm limit register
Register bit width: [7:0]
Offset: 0xD
Reset value: 0x60

Bit field	Bit field name	Bit width	Access	Description
[7:0]	EML	8	Rw	Error alarm threshold

23.4.9 RX Error Count Register (RXERR)

English name: RX error count register
Register bit width: [7:0]
Offset: 0xE
Reset value: 0x60

Bit field	Bit field name	Bit width	Access	Description
[7:0]	RXERR	8	R	Receive error count

23.4.10 TX Error Count Register (TXERR)

English name: TX error count register
Register bit width: [7:0]
Offset: 0xF
Reset value: 0x60

Bit field	Bit field name	Bit width	Access	Description
[7:0]	TXERR	8	R	Transmit error count

23.4.11 Acceptance filter

With the help of acceptance filter, only when the value predefined by identification bit and acceptance filter in received message are equal, can CAN controller be allowed to store the received message into RXFIFO. The acceptance filter is defined by acceptance code register and acceptance mask register. In mode register, the single filter mode or double filter mode is selected. See SJA1000 data manual for the specific configuration.

23.4.12 RX message count register (RMCR)

English name: RX message count register
Register bit width: [7:0]
Offset: 0x1 D
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
[7:0]	RMCR	8	R	The received data frame counter

23.5 Public Register

23.5.1 Bus timing register 0 (BTR0)

English name: Bus timing register
Register bit width: [7:0]
Offset: 0x06
Reset value: 0x00

Notes: in reset mode, it’s read and written; in operating mode, it’s read-only.

Bit field	Bit field name	Bit width	Access	Description
7: 6	SJW	8	RW	Synchronization skip width
[5£º0]	BRP	8	RW	The Baud rate frequency division factor

23.5.2 Bus timing register 1 (BTR1)

English name: Bus timing register 1
Register bit width: [7:0]
Offset: 0x07

Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
7	SAM	1	Rw	When the bit is 1, it's sampled three times, or sampled once.
6: 4	TESG2	3	Rw	The count value of time period 2 in a bit
3:0	TSEG1	4	Rw	The count value of time period 2 in a bit

23.5.3 Output Control Register (OCR)

English name: Output control register
Register bit width: [7:0]
Offset: 0x08
Reset value: 0x00

Bit field	Bit field name	Bit width	Access	Description
[7:0]	OCR	8	Rw	Reserved

24 ADC Controller

24.1 Overview

Loongson 1C integrates the ADC controller that is used to control ADC channel and has implemented some specific applications, such as continuous switch, single switch, touch screen application and analog watchdog.

Main characteristic parameters of ADC controller in Loongson 1C include:

- 4-channel ADC analog input, 10bit output precision
- Measuring voltage scope is 0.01~0.99VREF, and recommend the VREF input of 0.5~0.9VDDA
- The operating frequency of ADC can be configured from 0 to 16M
- The operating mode of ADC has single and continuous switch, and the touch screen application belong to the special continuous switch.
- The continuous conversion of ADC adopts DMA transmission data, but the coordinates of touch screen doesn't adopt DMA.
- The continuous conversion interval of ADC can be configured from 0 to 1M.
- In continuous switch, the unused channels of ADC may conduct the single switch.
- In touch screen application, when the touch screen is pressed, the interrupt is generated; when the touch screen is released, the interrupt is also generated.
- It can support four-wire touch screen and five-wire touch screen. In the connection of four-wire touch screen, two ways of general ADC may be used. In the connection of five-wire touch screen, three ways of general ADC may be used.
- Support multi-channel scanning single conversion
- It supports the function of analog watchdog, and the upper and lower thresholds may be configured. And the interrupt is generated when exceeding the threshold.

24.2 Register Description

Register name	Address	Read / Write (R / W)	Function description	Reset value
adc_cnt	0xbfe74000	R/W	Frequency division and sampling interval register	0x400010

Adc_cnt	Bit	Default values	Description
adc_pre	31:20	0x4	The frequency division value of adc conversion clock is from 0 to 16M, and the clock after frequency division is F= sys_clk/adc_pre
cc_gap	19:0	0x10	The interval count of continuous conversion is from 0 to 1M, and the clock count after frequency division is used.

Register name	Address	Read / Write (R / W)	Function description	Reset value
adc_s_ctrl	0xbfe74004	R/W	Single sampling control register	0x0

adc_s_ctrl	Bit	Default values	Description

reserved	31:7	0x0	
power_down	6	0x0	Stop ADC conversion, including all AD conversions Active high, turn off the power.
soft_reset	5	0x0	Soft reset; the high level is valid; the hardware is cleared automatically
soc	4	0x0	The conversion starts; the high level is valid; the hardware is cleared automatically
ch_s_sel	3:0	0x0	Single conversion channel selection, four bits correspond to four channels

Register name	Address	Read / Write (R / W)	Function description	Reset value
adc_c_ctrl	0xbfe74008	r/w	Continuous sampling control register	0x0

adc_c_ctrl	Bit	Default values	Description
reserved	31:8	0x0	
cc_en	7	0x0	Continuous switch enable. When the bit is 1, it's significant; when the bit is 0, the continuous conversion is disabled.
touch_pad_sel	6	0x0	Touch screen application enable. The touch screen is used when the bit is 1.
mode5_or_mode4	5	0x0	Four-wire or five-wire touch screen. Five-wire touch screen at 1; Four-wire touch screen at 0.
awatchdog_sel	4	0x0	Analog watchdog enable, significant at 1
ch_s_sel	3:0	0x0	Single conversion channel selection, four bits correspond to four channels

Register name	Address	Read / Write (R / W)	Function description	Reset value
x_range	0xbfe74010	r/w	Touch screen X direction threshold	0x3ff0000

x_range	Bit	Default values	Description
reserved	31:26	0x0	
x_range_max	25:16	0x3ff	The maximum threshold is x direction is used to judge whether the touch screen has been pressed.
reserved	15:10	0x0	
x_range_min	9:0	0x0	The minimum threshold of x direction is used to judge whether the touch screen has been pressed.

Register name	Address	Read / Write (R / W)	Function description	Reset value
y_range	0xbfe74014	r/w	Touch screen X direction threshold	0x3ff0000

y_range	Bit	Default values	Description
reserved	31:26	0x0	
y_range_max	25:16	0x3ff	The maximum threshold of y direction is used to judge whether the touch screen has been pressed.
reserved	15:10	0x0	
y_range_min	9:0	0x0	The minimum threshold of y direction is used to judge whether the touch screen has been pressed.

Register name	Address	Read / Write (R / W)	Function description	Reset value
awatchdog_range	0xbfe74018	r/w	Analog watchdog threshold	0x3f0000f

awatchdog_range	Bit	Default values	Description
reserved	31:26	0x0	
awcg_range_max	25:16	0x3f0	The maximum threshold of analog watchdog is used to judge whether the interrupt is generated.
reserved	15:10	0x0	
awcg_range_min	9:0	0xf	The minimum threshold of analog watchdog is used to judge whether the interrupt is generated.

Register name	Address	Read / Write (R / W)	Function description	Reset value
axis	0xbfe74020	ro	Touch screen coordinates	0x0

axis	Bit	Default values	Description
reserved	31:26	0x0	
x_axis	25:16	0x0	X coordinate of the touch screen
reserved	15:10	0x0	
y_axis	9:0	0x0	Y coordinates of the touch screen

Register name	Address	Read / Write (R / W)	Function description	Reset value
adc_s_dout0	0xbfe74024	ro	Single conversion result, channel 0 and channel 1	0x0

adc_s_dout0	Bit	Default values	Description
adc_busy	31	0x0	Switch to busy status and set the bit to 1 after writing soc. The hardware is cleared after all single conversions.
reserved	30:26	0x0	
adc_data1	25:16	0x0	Single conversion result of Channel 1
reserved	15:10	0x0	

adc_data0	9:0	0x0	Single conversion result of Channel 0

Register name	Address	Read / Write (R / W)	Function description	Reset value
adc_s_dout1	0xbfe74020	ro	Single conversion result, channel 0 and channel 1	0x0

adc_s_dout1	Bit	Default values	Description
adc_busy	31	0x0	Switch to busy status and set the bit to 1 after writing soc. The hardware is cleared after all single conversions.
reserved	30:26	0x0	
adc_data3	25:16	0x0	Single conversion result of Channel 3
reserved	15:10	0x0	
adc_data2	9:0	0x0	Single conversion result of Channel 2

Register name	Address	Read / Write (R / W)	Function description	Reset value
adc_c_dout	0xbfe74028	ro	Continuous conversion results	0x0

adc_c_dout	Bit	Default values	Description
reserved	31:26	0x0	
adc[i+1]	25:16	0x0	Conversion results of ADC[i+1] in continuous conversion
reserved	15:10	0x0	
adc[i]	9:0	0x0	Conversion results of ADC[i] in continuous conversion

Register name	Address	Read / Write (R / W)	Function description	Reset value
adc_debounce_cnt	0xbfe7402c	ro	Touch screen debouncing time	0x640

adc_debounce_cnt	Bit	Default values	Description
reserved	31:20	0x0	
debounce_cnt	19:0	0x640	Debouncing delay time

Register name	Address	Read / Write (R / W)	Function description	Reset value
adc_int	0xbfe74030	ro	ADC interrupt flag and control	0x0

adc_int	Bit	Default values	Description
reserved	31:10	0x0	
fifo_empty	9	0x0	fifo empty status in continuous conversion
fifo_full_int_en	8	0x0	In continuous conversion, fifo full interrupt

			enable. When the bit is 1, the interrupt is started; when the bit is 0, the interrupt is masked.
awcg_int_en	7	0x0	Analog watchdog interrupt enable. When the bit is 1, the interrupt is started; when the bit is 0, the interrupt is masked.
release_int_en	6	0x0	Touch screen released interrupt enable. When the bit is 1, the interrupt is started; when the bit is 0, the interrupt is masked.
press_int_en	5	0x0	Touch screen pressed interrupt enable. When the bit is 1, the interrupt is started; when the bit is 0, the interrupt is masked.
Fifo_full_int	4	0x0	In continuous conversion, fifo full interrupt status, the software writes 1 and is cleared 0
awcg_h_int	3	0x0	The voltage of analog watchdog exceeds the maximum threshold interrupt state, the software writes 1 and is cleared
awcg_l_int	2	0x0	The voltage of analog watchdog exceeds the minimum threshold interrupt state, the software writes 1 and is cleared
release_int	1	0x0	Touch screen released interrupt status. The software writes 1 and is cleared.
press_int	0	0x0	Touch screen pressed interrupt status. The software writes 1 and is cleared.

24.3 Configuration Operations

Before the ADC interface works normally, configure all registers need configuring. The configuration procedures of ADC controller are as follows:
1. Configure adc_int register, enable or disable the interrupt of ADC controller.
2. Configure time parameter register adc_cnt, set frequency division factor and interval of continuous conversion.
3. If there is touch screen application, configure adc_debounce_cnt, and set the pressed or released debouncing time; in addition, thresholds in X and Y directions are configured to judge whether the interrupt is generated.
4. If there is analog watchdog application, configure the awatchdog_range register, and the watchdog threshold.
5. Configure adc_c_ctrl register, set the application mode (such as touch screen application and analog watchdo) and continuous conversion channel.
6. Configure adc_s_ctrl register, set the single conversion channel, start and stop conversion.
7. Result-reading register. The single conversion result is stored in adc_s_dout0 and adc_s_dout1; the coordinates of touch screen are stored in axis; the result of continuous conversion read adc_c_dout register via DMA.
Notes: after the continuous conversion starts, the conversion won't stop unless adc_c_ctrl[7] is configured to 0. If it's necessary to change the continuous conversion channel, stop the continuous conversion first, and start the conversion again after the reconfiguration of channels. If it's necessary to insert the single conversion during continuous conversion (the single conversion can't be done in the used continuous conversion channel), and it's not necessary to stop the continuous conversion. The results of each continuous conversion will replace the previous value, so the touch screen coordinates axis and adc_c_dout must be read promptly.
In addition, in general ADC continuous conversion, the corresponding relationship of channel selection and adc_c_dout output is shown in the table below. For example, ch_c_sel[3:0]=b, select ADC0, ADC1 and ADC3 continuous conversion, the ADC0 data are put in adc_c_dout[9:0] of the first word, the ADC1 data put in adc_c_dout[25:16] of the first word, and the ADC3 data put in adc_c_dout[9:0] of the second word.

ch_c_sel[3:0]	ch[0]	ch[1]	ch[2]	ch[3]
1	Dout0[9:0]			
2		Dout0[9:0]		

3	Dout0[9:0]	Dout0[25:16]		
4			Dout0[9:0]	
5	Dout0[9:0]		Dout0[25:16]	
6		Dout0[9:0]	Dout0[25:16]	
7	Dout0[9:0]	Dout0[25:16]	Dout1[9:0]	
8				Dout0[9:0]
9	Dout0[9:0]			Dout0[25:16]
a		Dout0[9:0]		Dout0[25:16]
b	Dout0[9:0]	Dout0[25:16]		Dout1[9:0]

c)			Dout0[9:0]	Dout0[25:16]
d	Dout0[9:0]		Dout0[25:16]	Dout1[9:0]
e		Dout0[9:0]	Dout0[25:16]	Dout1[9:0]
f	Dout0[9:0]	Dout0[25:16]	Dout1[9:0]	Dout1[25:16]

The sequence diagram of inserting single conversion in continuous conversion is shown as follows:

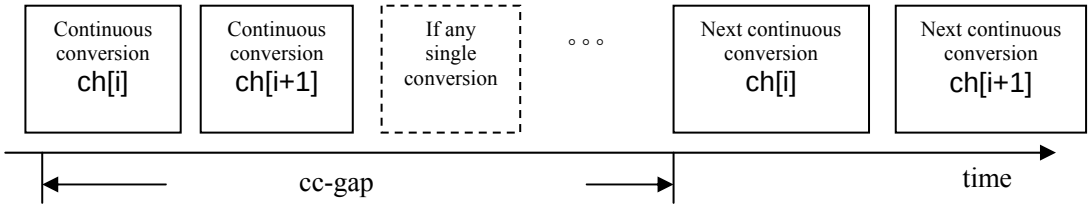

Figure 24-1 Schematic diagram of ADC single conversion/continuous conversion

If the cc_gap interval is not long enough for inserting one single conversion, it will cause the timing of the next continuous conversion move backwards, which should be noted in software configuration of cc_gap.

25 PWM Controller

25.1 Overview

Loongson 1C has implemented the four-way pulse width adjustment/count controller (hereinafter referred to as PWM), and each way of PWM work and control mode are the same. Each PWM has one way pulse width output signal (pwm_o)). The system clock is up to 100MHz, and count register and parameter register are all 24bits data width.
The base address of the four-way PWM controller system is shown as follows:

Table 25-1 Four-channel controller description

Name	Base address
PWM0	0xbfe5_c000
PWM1	0xbfe5_c010
PWM2	0xbfe5_c020
PWM3	0xbfe5_c030

Each way of controller has four control registers in total as follows:

Table 25-2 Control register description

Name	Address	Width	Access	Note
CNTR	Base + 0x0	24	R/W	Basic counter
HRC	Base + 0x4	24	R/W	High pulse timing reference register
LRC	Base + 0x8	24	R/W	Low pulse timing reference register
CTRL	Base + 0xC	8	R/W	Control register

25.2 PWM Register Description

Implement pulse width function

CNTR register can be written in by system programming to obtain the initial value, and after the system programming and writing, driven by system clock CNTR register will add continuously, and is cleared after reaching the value of LRC register. Then, it will start to add continuously, and the controller produces the continuous pulse width output.

Table 25-3 Basic counter settings

CNTR	Bit field	Access	Reset value	Note
Reserved	31:24	R/W	0x0	
CNTR	23:0	R/W	0x0	Basic counter count value. After the counter starts to work (CTRL[0] is 1), after counted to Lvalue, the counter is cleared. If CTRL[4] is 0, the counter starts to count from start; if CTRL[4] is 1, the counter stops.

HRC register is written in by system, and when the value of CNTR register is equal to HRC value, controller generates high level pulse.

Table 25-4 High pulse count threshold settings

Hvalue	Bit field	Access	Reset value	Note
Reserved				
Hvalue	23:0	R/W	0x0	High pulse count threshold.

				When the counter counts to the threshold, output high level (it's necessary to configure CTRL[3] to 0)

LRC register is written in by system, and when the value of CNTR register is equal to LRC value, the controller will generate low pulse level.

Table 25-5 Low pulse count threshold settings

Lvalue	Bit field	Access	Reset value	Note
Reserved				
Lvalue	23:0	R/W	0x0	Low pulse count threshold. When the counter counts to the threshold, the low level is output.

For example, if the width to be generated has been the high pulse width 50 times system clock cycle and low pulse width 90 times system clock cycle. In HRC, the initial value should be configured as (90-1)=89, and in LRC register, the initial value configured as (50+90-1)=139

When working in timer mode, CNTR records the internal system clock, and the initial value of HRC and LRC registers are written in by system programming. When the value of CNTR register is equal to HRC or LRC, the chip will generate an interrupt, and the timer function is implemented thereby.

In three operating modes of CTRL control register, the function of control register remains unchanged, and different configurations are selected based on functional requirement.

Table 25-6 Control register settings

CTRL	Bit field	Access	Reset value	Description
INT_LRC_EN	11	R/W	0	Low pulse counter interrupt enable Set 1: when the INTEN is 1, the interrupt is generated after the CNTR counts to LRC. Set to 0: no interrupt is generated
INT_HRC_EN	10	R/W	0	High pulse counter interrupt enable Set 1, when the INTEN is 1, CNTR an interrupt is generated after CNTR counts to HRC, Set to 0: no interrupt is generated
Reserved	9:8	R/W	0	
CNTR_RST	7	R/W	0	Make CNTR counter clear Set to 1: CNTR counter is cleared Set 0: the CNTR counter works normally
INT_SR	6	R/W	0	Interrupt status bit Read operation: 1 represents that the interrupt occurs; 0 represents no interrupt Write in 1: Clear interrupt
INTEN	5	R/W	0	Interrupt enable bit Set 1: interrupt enable. Only when the bit is 1 and meets the interrupt conditions of high pulse or low pulse, the interrupt occurs. Set to 0: no interrupt is generated
SINGLE	4	R/W	0	Single pulse control bit Set to 1: generate pulse only once Set to 0: continue to generate pulse,

OE	3	R/W	0	pulse output enable control bit, active low Set to 0: pulse output enable Set to 1: pulse output mask
Reserved	2: 1	R/W	2'b0	Reserved
CNT_EN	0	R/W	0	Basic counter enable bit Set to 1: CNTR to count Set to 0: CNTR stops counting

26 Watchdog (WDT)

26.1 Overview

In the system, the WDT (Watchdog Timer) is actually a counter. Generally, a large number is assigned to the Watchdog, and the Watchdog starts to count down after the system runs. If the program works normally, later the CPU should send out command to make the Watchdog reset and restart to count down. If the Watchdog reduces to 0, the program is considered to work abnormally, and the entire system is forced to reset. The figure below is the implementation of Watchdog, and the system configuration of Watchdog. The Watchdog has one counter inside, and the internal comparator compares if the counter value is zero. If it's zero, it will send the soft reset signal to restart the system.

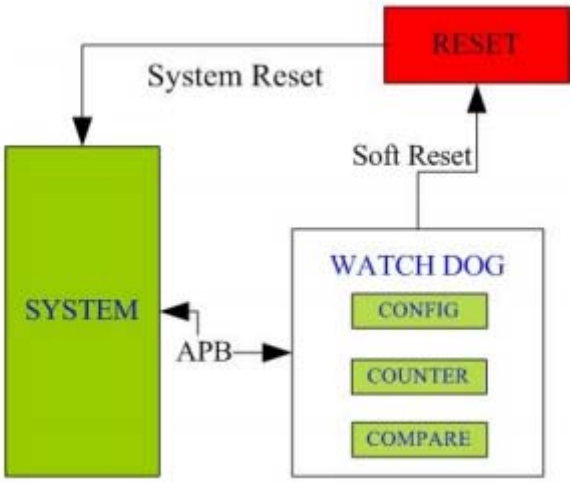

Figure 26-1 Watchdog architecture chart

26.2 Description of WATCHDOG Register

The Watchdog logic mainly has three programmable registers, and the base address is Those formations are described as follows:

26.2.1 Watchdog Enable Register (WDT_EN)

Address: 0xbfe7_c060

Bit	Bit field name	RW (read/write)	Description
31:1			Reserved
0	WDT_EN	R/W	Watchdog enable

26.2.2 Watchdog Set Register (WDT_SET)

Address: 0xbfe7_c068

Bit	Bit field name	RW (read/write)	Description
31:1			Reserved
0	WDT_SET	R/W	Watchdog counter setting

26.2.3 Watchdog Timer (WDT_timer)

Address: 0xbfe7_c064

Bit	Bit field name	RW	Description
31:0	WDT_timer	R/W	Watchdog counter value

The setup sequence of such three registers in system: the system first configures the Watchdog enable bit WDT_EN; then, it configures the initial value of Watchdog starts timer WDT_TIMER, and the value has been stored in a special register; after the system sets WDT_SET, the counter begins to count.
The Watchdog hasn't implemented the function of low consumption, and its operation has nothing to do with the hardware design. If the Watchdog is required to operate, the software needs to update the counter value timely.

27 High-precision Timer (HCNTR)

27.1 Overview

1C2 chip adds a high-precision timer inside, adopts 1M clock count, and may generate the cyclic interrupt output by 1us at least and 2^{31}us at most based on configuration register. The timer clock is from external oscillator, and isn't affected by the chip operating frequency. When the system implements the dynamic undeclocking, it provides the steady clock.

27.2 Register Description

Register name	Address	RW (read/write)	Function description	Reset value
hcntr_ctrl	0xbfe74028	r/w	CNTR control register	0x0

hcntr_ctrl	Bit	Default values	Description
cnt_en	31	0x0	Counter enable. When the bit is 1, the counter starts to count. When the bit is 0, the counter stops counting
Reserved	30:5	0x0	
int_prd	4:0	0x0	Timer interrupt period The interrupt cycle is 2^{int_prd}us

Register name	Address	RW (read/write)	Function description	Reset value
hcntr_cntr	0xbfe74028	ro	CNTR counter value	0x0

hcntr_ctrl	Bit	Default values	Description
Reserved	31:20	0x0	
hcntr_cntr	19:0	0x0	Timer count value for the current count

The timer can only implement the cycle timing by powers of 2, such as 1, 2, 4, 8 and16us. For example, if int_prd is configured to 5, the interrupt cycle is 2^5=32us.